ANALOG DEVICES

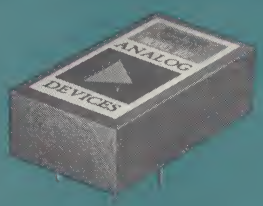
A COMPLETE LINE OF OPERATIONAL AMPLIFIERS FOR INSTRUMENTATION, COMPUTATION AND CONTROL.

Low Cost Differential

MODEL 106 — $26.

Gain — 1.5×10^5; Voltage Drift — 20uV/°C; Current Drift — 1.5na/°C; Output — ±10V @ 5ma;-Input Impedance — 50 MΩ, CM; Bandwidth — 1.5mc;

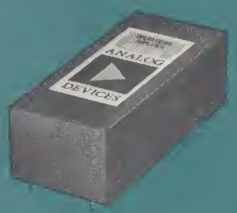
Fast Response Differential Inverting and NonInverting



MODEL 102 — 10MC AND 30V/ USEC

Gain — 10^6; Voltage Drift — 5uV/°C; Current Drift—0.4na/°C; Output — ±11V @ 20 ma; Input Impedance — 500 MΩ, CM; Full Output Response — 300KC

Ultra Low Voltage Drift Chopper Stabilized



MODEL 202 — 0.2uV/°C

Current Drift — 0.5pa/°C; Gain — 10^9; Bandwidth — 10mc; Overload Recovery — 0.5usec; Output — ±11V @ 20ma; Slew Rate — 30V/usec; Internal Chopper Drive

Ultra Low Input Current with High Input Impedance

MODEL 301 — 1PA AND 10^{12} OHMS

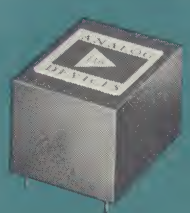
Current Drift — 0.06pa/°C; Noise — 1uV and 0.01pa; Voltage Drift — 30uV/°C; Gain — 10^6; Output — ±10V @ 20ma; Common Mode Voltage — ±300V

Low Cost — Fast Slew Rate Chopper Stabilized

MODEL 210 — $157. AND 100V/ USEC

Voltage Drift — 1uV/°C; Current Drift — 2pa/°C; Bandwidth — 20mc; Voltage Noise — 3uV; Output — ±10V @ 20ma; Overload Recovery — 0.2usec; Internal Chopper Drive

High Output Current



MODEL 116 — ±11V AND 100MA

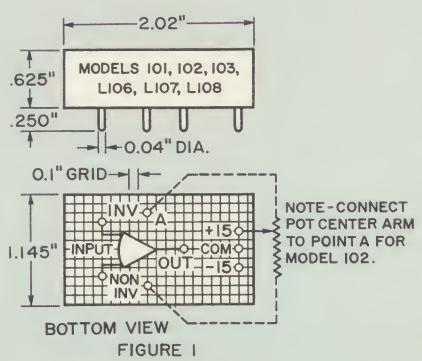
Bandwidth — 10mc; Full Output Response — 500KC; Gain — 10^5; Noise — 3uV; Slew Rate — 30V/usec; Overload Recovery — 0.2usec; Fast Response on Non-Invertor

ALL SILICON, SOLID-STATE OPERATIONAL AMPLIFIERS

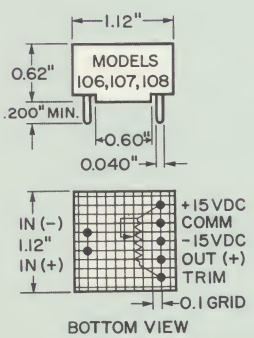
	HIGH PERFORMANCE DIFFERENTIAL			LOW COST DIFFERENTIAL		
	Excellent time drift, low initial voltage offset, high input impedance, low input current, high gain and selection of voltage drifts to 5uV/°C			For greatest economy without the usual sacrifice in gain, drift and output current. AC gain of 94db to 1KC on 106/107.		
SPECIFICATIONS (typical @ 25°C unless otherwise noted.)	**101 A/B/C** Wideband Inverting ±8 to 16V Power Supply 5ma Output Current	**102 A/B/C** Wideband NonInverting Very High Gain—20ma Fast Slewing Rate	**103 A/B/C** Low Frequency 20ma Output Current ±8 to 16V Power Supply	**106/L106** 5ma Output Current High Gain Excellent AC ampl.	**107/L107** 5ma Output Current High Gain Reduced Input Current	**108/L108** Low Frequency Lowest Input Current High Input Impedance
OPEN LOOP GAIN @ DC, rated load, min.	10^5	2×10^6	10^5	1.5×10^5	1.5×10^5	5×10^4
RATED OUTPUT						
Voltage, min.	±11V	±11V	±11V	±10V	±10V	±10V
Current, min.	5ma.	20ma.	20ma.	5ma.	5ma.	2.5ma
FREQUENCY RESPONSE						
Unity gain, small signal	10mc	10mc	500KC	1.5mc	1.5mc	500KC
Full Output Voltage	30KC	300KC	2KC	20KC	20KC	2KC
Slewing Rate	2V/μsec	30V/μsec	0.13V/μsec	1.2V/μsec	1.2V/μsec	0.12V/μsec.
Overload Recovery	200μsec	—	5msec.	1msec	1msec	5msec
INPUT VOLTAGE OFFSET						
Initial Offset, @ 25°C, max.[1]	±1mV	±1mV	±1mV	—	—	—
Avg. vs. temp., max.[5]	Models A — 20μV/°C, B — 10μV/°C, C — 5μV/°C			20μV/°C	20μV/°C	20μV/°C
vs. supply voltage, max.	15μV/%	10μV/%	15μV/%	20μV/%	20μV/%	20μV/%
vs. time	10μV/day	10μV/day	10μV/day	50μV/day	50μV/day	50μV/day
INPUT CURRENT OFFSET						
Initial Offset, @ 25°C, max.	±2na	±2na	±2na	±150na	±20na.	±2na
Avg. vs. temp., max.[5]	0.2na/°C	0.4na/°C	0.2na/°C	1.5na/°C	1.5na/°C	0.3na/°C
vs. supply voltage, max.	0.15na/%	0.15na/%	0.15na/%	2na/%	2na/%	0.3na/%
INPUT IMPEDANCE						
Between Inputs	4MΩ	6MΩ	4MΩ	100KΩ	100KΩ	4MΩ
Common Mode	500MΩ	500MΩ	500MΩ	50MΩ	50MΩ	500MΩ
INPUT VOLTAGE						
Max. Between Inputs	±15V	±15V	±15V	±15V	±15V	±15V
Max. Common Mode	±10V	±10V	±10V	±10V	±10V	±10V
Common Mode Rejection	20,000	20,000	20,000	20,000	20,000	20,000
INPUT NOISE						
Voltage, DC to 1CPS, P to P	—	—	—	—	—	—
5 to 50KC, RMS	4μV	8μV	4μV	4μV	4μV	4μV
Current, DC to 1CPS, P to P	—	—	—	—	—	—
POWER SUPPLY						
Voltage	±(8 to 16) VDC[2]	±(15 to 16) VDC	±(8 to 16) VDC[2]	±(15 to 16) VDC	±(15 to 16) VDC	±(15 to 16) VDC
Current, rated load	20ma.	35ma.	30ma.	15ma.	15ma.	5ma.
CASE SIZE	Fig. 1	Fig. 1	Fig. 1	Fig. 2/Fig. 1	Fig. 2/Fig. 1	Fig. 2/Fig. 1

PRICE	A	B	C	A	B	C	A	B	C	106	L106	107	L107	108	L108
1-9	$68	78	98	95	105	120	74	84	104	26	30	31	35	35	40
10-24	$66	75	95	92	102	116	71	81	101	25	29	30	34	33	37

ANALOG DEVICES



BOTTOM VIEW
FIGURE 1

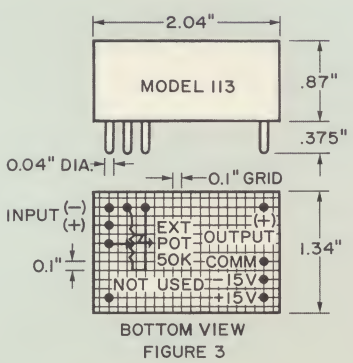


BOTTOM VIEW
FIGURE 2

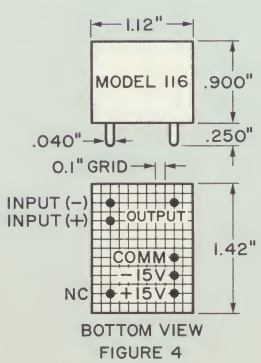
Note 1 — Offset within specified limits with no external adjustment. All units adjustable to zero external pot.

Note 2 — Specifications given for ±15VDC

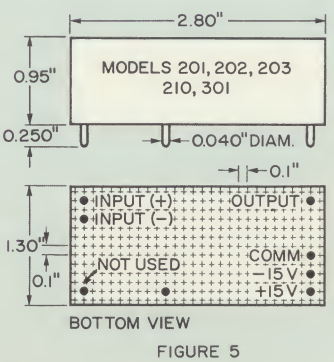
HIGH OUTPUT CURRENT		CHOPPER STABILIZED				ULTRA LOW INPUT CURRENT
Output current of 100ma and bandwidth to 10mc drives galvonometers and coaxial cables.		Miniature encapsulated modules for P.C. mounting or plug-in sockets. Includes internal chopper drive and fast overload recovery circuitry. Very high gains and output current.				
113 **High Gain** **Low Drift** **High Input Impedance**	**116** **Low Noise** **Excellent AC ampl.** **Fast Recovery**	**201** **100ma Output Current** **Wideband** **Ultra Low Drift**	**202** **Wideband — 20ma** **Fast Slew Rate** **Ultra Low Drift**	**203** **Low Noise — 20ma** **Low Frequency** **Ultra Low Drift**	**210** **Low Cost — 20ma** **Very Fast Slew Rate** **Low Noise**	**301** **High CM Voltage** **Very High Zin** **Very Low Noise**
2×10^6	10^5	10^9	10^9	10^8	10^8	10^6
±11V 100ma	±11V 100ma.	±11V 100ma.	±11V 20ma.	±11V 20ma.	±10V 20ma.	±10V 20ma.
10mc 300KC 30V/μsec —	10mc 500KC 30V/μsec 0.2μsec	10mc 500KC 30V/μsec 0.5μsec.	10mc 500KC 30V/μsec 0.5μsec.	2mc 20KC 1.2V/μsec 5μsec.	20mc 500KC 100V/μsec 0.2μsec.	500KC 5KC 0.3V/μsec 200μsec
±1mV 20μV/°C 2μV/% 10μV/day	±10mV 100μV/°C — —	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±100μV 1μV/°C[6] 10μV/% 1μV/day	— 30μV/°C 30μV/% —
±1na 0.2na/°C —	±300na. 40na/°C —	50pa 0.5pa/°C[3] 1pa/%	50pa 0.5pa/°C[3] 1pa/%	50pa 0.5 pa/°C[3] 1pa/%	100pa. 2pa/°C 10pa/%	±1pa 0.3pa/°C[4] .001pa/%
7.5MΩ 500MΩ	20KΩ 2.5MΩ	220KΩ N.A.	220KΩ N.A.	220KΩ N.A.	500KΩ N.A.	10^{10}Ω, 500pf 10^{12}Ω, 10pf
±15V ±10V 100,000	±15V ±10V —	±15V single ended	±15V single ended	±15V single ended	±15V single ended	±20V ±300V 10^8
— 8μV —	— 3μV —	25μV 10μV 20pa	25μV 10μV 20pa	10μV 10μV 10pa	5μV 10μV 10pa	1μV — .01pa
±(15 to 16) VDC 150ma.	±(15 to 16) VDC 150ma.	±(15 to 16) VDC 150ma.	±(15 to 16) VDC 50ma.	±(15 to 16) VDC 50ma.	±(15 to 16) VDC 60ma.	±(15 to 16) VDC 35ma.
Fig. 3	Fig. 4	Fig. 5	Fig. 5	Fig. 5	Fig. 5	Fig. 5
195 185	98 95	270 256	235 224	215 205	157 148	198 193



BOTTOM VIEW
FIGURE 3



BOTTOM VIEW
FIGURE 4



BOTTOM VIEW
FIGURE 5

Note 3 — Maximum operating and storage temperature is 75°C

Note 4 — 0.06pa/°C from 0 to 50°C

Note 5 — Averaged over — 25 to + 85°C at each input

Note 6 — 2μV/°C from —25 to +10°C

ANALOG DEVICES

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2543 Industrial Boulevard
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305/293-5202

Holiday Office Center, Suite 11
Huntsville, Alabama
205/881-3294

5003 Brook Road
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703/266-2060

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315/454-9314

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303/936-3456

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2422 Camino Way
Salt Lake City, Utah
801/278-4465

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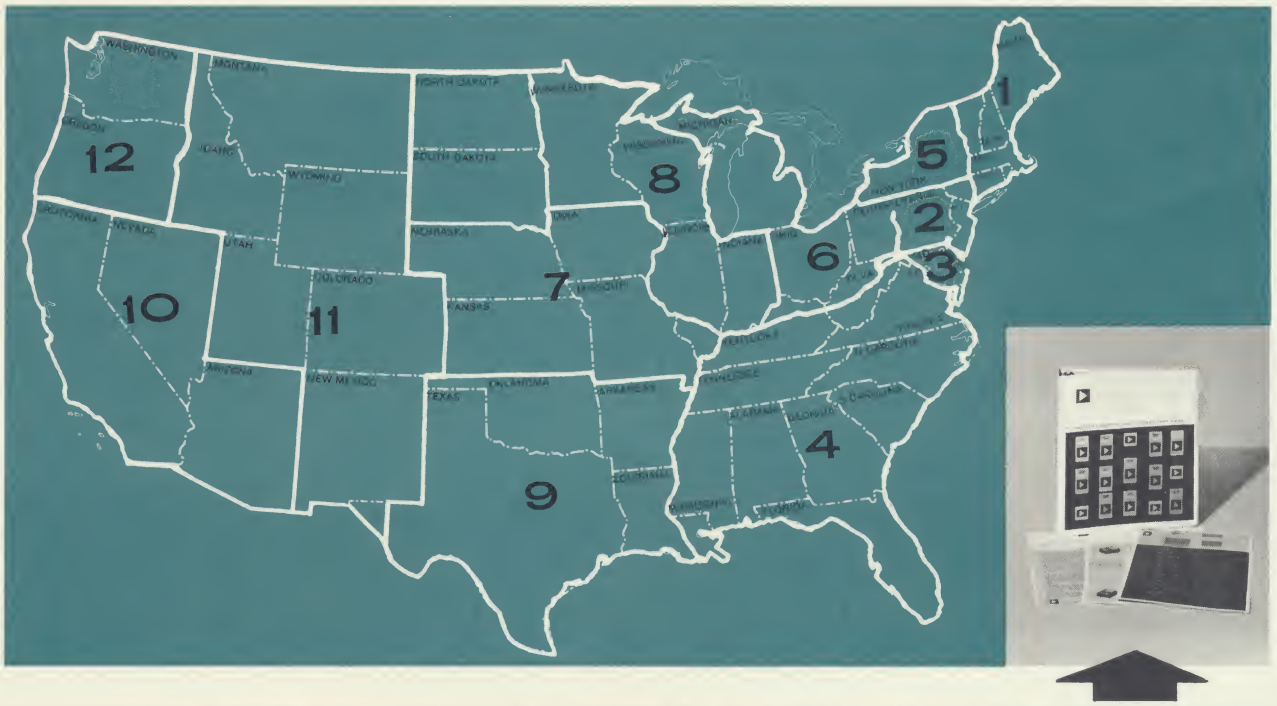
Avionics Liaison, Inc.
6770 Perimeter Road
Seattle, Washington
206/PA 3-7602



APPLICATION NOTES AND COMPLETE SPECIFICATION SHEETS AVAILABLE UPON REQUEST.

Cat. 2-66-SF

GENERAL COMPUTERS, INC.

* * * * * * THE PLUS FEATURES OF COMPUTING AND CONTROL AMPLIFIERS BY GENERAL COMPUTERS, INC. * * * * * *

This is the second in a series of technical bulletins being prepared by GENERAL COMPUTERS, Inc. to acquaint engineers and scientists with standard equipment available to them for computing and data processing. The purpose of this particular bulletin is to describe some of the outstanding features of the amplifiers manufactured by GENERAL COMPUTERS, Inc.

DRIFT - WHAT DOES IT MEAN?

First let us make a general note relative to specifications on drift. When GENERAL COMPUTERS, Inc. quotes a figure on drift it means that every amplifier sold will meet or exceed this performance level as received by the customer, without adjustment or calibration! Some companies quote a drift figure representing the change in performance that occurs after installing the amplifier and adjusting the drift to zero at the beginning of the measurement period. Naturally, a very low drift figure can be quoted under these idealized circumstances. But few users of equipment want to make continual adjustments to their equipment. As a result, the equipment seldom provides the performance quoted in the specifications. By contrast, the amplifiers manufactured by GENERAL COMPUTERS, Inc. are designed to be installed and operated without adjustment or calibration controls. They are designed to provide the performance specified for the life of the amplifier without requiring attention on the part of the operator. (Except, of course, in the event of a component failure.) Of course, if the user wishes to provide adjustments he can abtain even better performance from the amplifier than the specified values, especially lower drift.

DRIFT - AND ITS RELATION TO SHIELDING

The two main causes of drift of a chopper stabilized operational amplifier are the input offset of the chopper amplifier and the input offset of the DC amplifier. First, relative to the chopper amplifier: The circuits used by GENERAL COMPUTERS, Inc. and most other manufacturers of high quality chopper amplifiers are similar. However, there is a vast difference in the mechanical design of various amplifiers. Some other amplifiers are constructed in non-metalic cases. These non-metalic cases do not provide adequate shielding for the amplifier. External fields cause signal pickup which results in input offset, or drift, of the amplifier. This effect is easily observed as a change in balance of the amplifier when the hand is placed around the case. All GENERAL COMPUTERS, Inc. amplifiers are constructed in metal cases which provide proper shielding. Some other amplifiers have the components "haywired" into place. This type of construction results in variation of component placement from unit to unit, causing variations in performance. Also, repair of such units is made very difficult by crowding of parts and lack of terminal boards. GENERAL COMPUTERS, Inc. amplifiers all have their components mounted to terminals for uniformity and for ease of maintainance.

DRIFT - AND ITS RELATION TO BALANCED CIRCUITS.

The effect upon drift of the input offset of the DC section of a chopper stabilized amplifier is ofter ignored. Yet this factor can often result in drift greater than that specified for the complete chopper stabilized amplifier. The majority of DC amplifiers do not employ a true balanced input stage. One tube section is used as an amplifier and the other tube section operates as a cathode follower. This results in a variation of input offset, or drift, as tubes age or power supplies drift. (Especially heater power which seldom is regulated.) Such amplifiers normally require a bias of about one volt at the balance input terminal. This bias must be supplied by the chopper amplifier, which then requires an offset at the summing junction to produce this bias. With a gain of 1000 in the chopper amplifier, an offset of .001 volts is required to produc the bias required by the DC amplifier. NOTE THAT THIS IS TEN TIMES THE OFFSET LEVEL OF .0001 VOLTS CLAIMED FOR MOST CHOPPER STABILIZED AMPLIFIERS. The GENERAL COMPUTERS, Inc. DC amplifiers employ true balanced inputs. Each half of a dual triode is operated at the same voltages and currents. The resulting bias at the balance input is less than 0.1 volts. Reduced sensitivity to power supply shifts is realized.

GAIN - ITS PURPOSE AND ITS STABILITY

The open loop gain of an operational amplifier is a measure of the accuracy with which its transfer function will follow the ratio of output to input impedances. Consider two amplifiers delivering 100 volts output, one with an open loop gain of 10,000 and the other with an open loop gain of 100,000.(not including the gain of the chopper amplifier) The first amplifier requires .010 volts at its summing junction to produce 100 volts out. The second amplifier requires only .001 volts at its summing junction. This voltage at the summing junction represents an error equivalent to drift, in a dynamic sense. Note that this is often much greater than the DC offset which is generally quoted. The advantage of high gain is obvious.

The high gain of GENERAL COMPUTERS, Inc. amplifiers is obtained without resorting to the use of positive feedback. This means that the gain is much less sensitive to variations due to tube ageing. The specified gain is based upon nominal values of tube gain, to allow for normal tube ageing.

SUMMARY

In summary, GENERAL COMPUTERS, Inc. amplifiers are the finest designs presently available, in terms of circuitry performance, packaging and convenience of operation. They are well worth their price, especially when a realistic evaluation is made of the true performance that the user will get in his facility.

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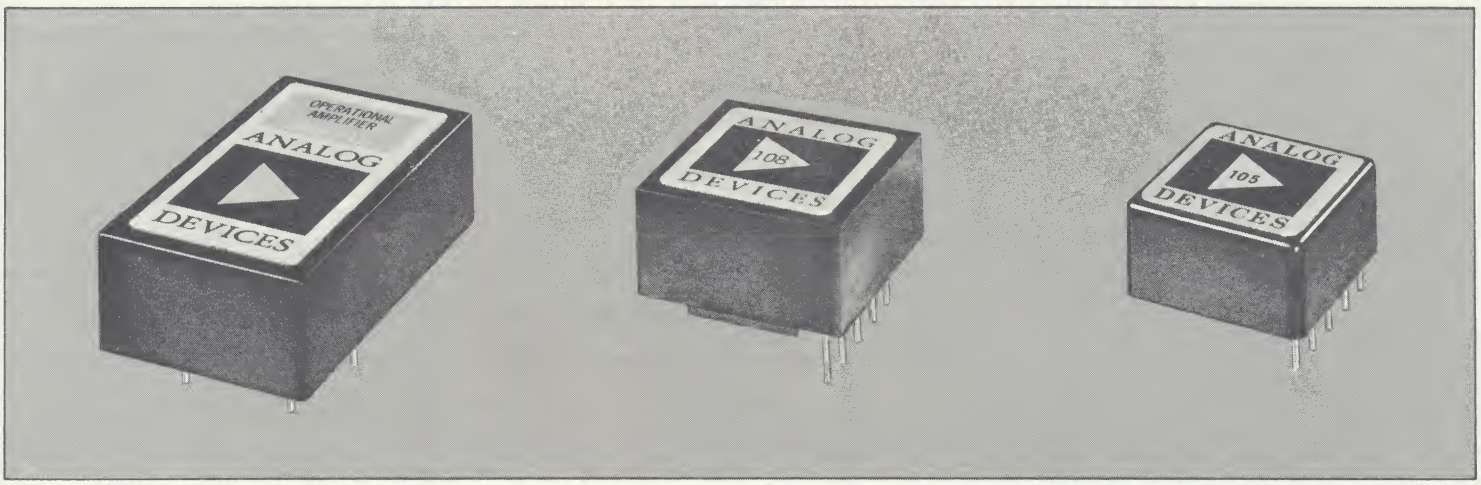
Economy Line Operational Amplifiers

.... a complete choice of "creative values" in operational amplifiers



See specifications inside for 8 new operational amplifier values

- ☐ **MODEL 105** — small size, good all around value — $19.
- ☐ **MODEL 106** — high voltage gain, 150,000 — $26.
- ☐ **MODEL 108** — low offset current, 0.3na/°C — $35.
- ☐ **MODEL 109** — high output current, ±10V @ 20ma — $55.
- ☐ **MODEL 110** — wideband, 20mc and 1mc full output — $58.
- ☐ **MODEL 140** — FET input, 100pa offset current — $85.
- ☐ **MODEL 160** — high output voltage, ±20V @ 2.5ma — $45.
- ☐ **MODEL 161** — high output voltage and current, ±20V @ 10ma — $65.

ANALOG DEVICES

Economy Line Operational Amplifiers

...your best value in operational amplifiers

SPECIFICATIONS (typical @ 25°C unless otherwise noted)	**Model 105** Miniature Size Lowest Cost	**Model 106/L106** High Gain 5ma Output	**Model 107/L107** High Gain 5ma Output	**Model 108/L108** Low Current Drift 0.3na°/C	**Model L109** High Output Current ±10V @ 20 ma
OPEN LOOP GAIN, rated load, min.	30,000	150,000	150,000	50,000	150,000
RATED OUTPUT, min.	±10V @ 2.2ma	±10V @ 5ma	±10V @ 5ma	±10V @ 2.5ma	±10V @ 20ma
FREQUENCY RESPONSE					
Unity gain, small signal	1.5mc	1.5mc	1.5mc	0.5mc	1.5mc
Full Power Response, min.	20KC	20KC	20KC	2KC	20KC
Slewing Rate, min.	1.2V/μsec	1.2V/μsec	1.2V/μsec	0.12V/μsec	1.2V/μsec
Overload Recovery	1msec	1msec	1msec	5msec	1msec
INPUT VOLTAGE OFFSET					
Initial Offset Ext. Trim Pot	50KΩ	50KΩ	50KΩ	250KΩ	50KΩ
vs. temp. (−25 to 85°C), max. avg.[1]	±20μV/°C	±20μV/°C	±20μV/°C	±20μV/°C	±20μV/°C
vs. supply voltage	±20μV/%	±20μV/%	±20μV/%	±20μV/%	±20μV/%
vs. time	±50μV/day	±50μV/day	±50μV/day	±50μV/day	±50μV/day
INPUT CURRENT OFFSET (ea. input)					
Initial Offset, 25°C, max.	(0, +)150na	(0, +)150na	±20na	±2na	±20na
vs. temp. (−25 to 85°C), max. avg.	±1.5na/°C	±1.5na/°C	±1.5na/°C	±0.3na/°C	±1.5na/°C
vs. supply voltage	±2na/%	±2na/%	±2na/%	±0.3na/%	±2na/%
INPUT CURRENT OFFSET (differential)					
Initial Offset, 25°C, typ.[2]	±20na	±20na	±20na, max.	±2na, max.	±20na, max.
vs. temp. (−25 to 85°C), typ.[2]	±0.5na/°C	±0.5na/°C	±0.5na/°C	±0.1na/°C	±0.5na/°C
INPUT IMPEDANCE					
Between Inputs	150KΩ	150KΩ	150KΩ	4MΩ	150KΩ
Common Mode	50MΩ	50MΩ	50MΩ	500MΩ	50MΩ
INPUT VOLTAGE and NOISE					
Volt. Between Inputs Absolute Max.	±15V	±15V	±15V	±15V	±15V
Max. Common Voltage	±10V	±10V	±10V	±10V	±10V
Voltage Noise, to 50KC; rms	4μV	4μV	4μV	4μV	4μV
POWER SUPPLY					
Voltage	±(15 to 16)VDC	±(15 to 16)VDC	±(15 to 16)VDC	±(15 to 16)VDC	±(15 to 16)VDC
Current, Quiescent[3]	4.5ma	8ma	8ma	6ma	8ma
TEMPERATURE RANGE					
Operating	−40 to 85°C	−40 to 85°C	−40 to 85°C	−40 to 85°C	−40 to 85°C
Storage	−55 to 125°C	−55 to 125°C	−55 to 125°C	−55 to 125°C	−55 to 125°C
PRICE		106 L106	107 L107	108 L108	
(1-9)	$19	$26 30	$31 35	$35 40	$55
(10-24)	$18	$25 29	$30 34	$33 37	$52
CASE SIZE	Fig. 1	Fig. 2/Fig. 3	Fig. 2/Fig. 3	Fig. 2/Fig. 3	Fig. 3

Footnotes:

1. may be selected to 10μv/°C at slight additional cost, except model 140
2. may be guaranteed as max. limits on special order
3. add load and feedback current to obtain power supply drain
4. offset current doubles each 10°C, max. offset at 85°C is 10na

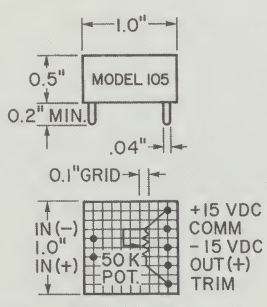


FIGURE 1 BOTTOM VIEW
Mating socket AC1003

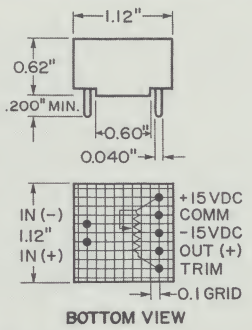
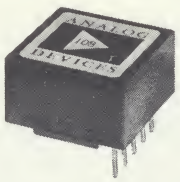
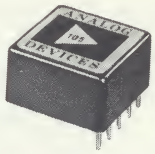


FIGURE 2 BOTTOM VIEW
Mating socket AC1003

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	Model 110 Wideband Fast Slew Rate	Model 140 F.E.T. Input 100pa Offset Current	Model 160 High Output Voltage ±20V @ 2.5ma	Model L161 High Output Voltage ±20V @ 10ma
	50,000	50,000	150,000	150,000
	±10V @ 20ma	±10V @ 2.2ma	±20V @ 2.5ma	±20V @ 10ma
	20mc (inv.) 1mc (inv.) 100V/μsec 100 μsec	1.5mc 20KC 1.2V/μsec 1msec	1.5mc 20KC 1.2V/μsec 1msec	1.5mc 20KC 1.2V/μsec 1msec
	100KΩ ±20μV/°C ±40μV/% ±50μV/day	1KΩ ±30μV/°C ±30 μV/% ±50μV/day	200KΩ ±20μV/°C ±20μV/% ±50μV/day	200KΩ ±20μV/°C ±20μV/% ±50μV/day
	(0, +)75na ±1na/°C ±1na/%	(0, +)100pa 10na⁴/110°C ±1pa/%	±20na ±1.5na/°C ±2na/%	±20na ±1.5na/°C ±2na/%
	inverting only	— —	±20na, max. ±0.5na/°C	±20na, max. ±0.5na/°C
	1MΩ N.A.	10^{11}Ω 10^{12}Ω	150KΩ 50MΩ	150KΩ 50MΩ
	±15V N.A. 4μV	±10V ±10V 8μV	±20V ±10V 4μV	±20V ±10V 4μV
	±(15 to 16)VDC 8ma	±(15 to 16)VDC 5ma	±(23 to 25)VDC 5ma	±(23 to 25)VDC 8ma
	−40 to 85°C −55 to 125°C	−25 to 85°C −55 to 85°C	−40 to 85°C −55 to 125°C	−40 to 85°C −55 to 125°C
	$58 $55	$85 $81	$45 $42	$65 $62
	Fig. 2	Fig. 2	Fig. 2	Fig. 3

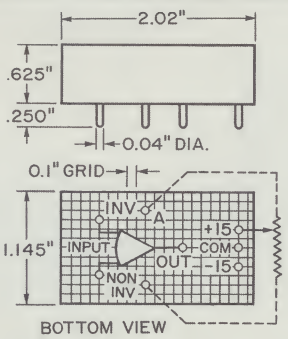
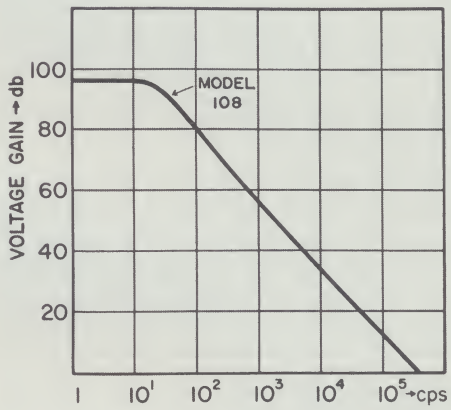
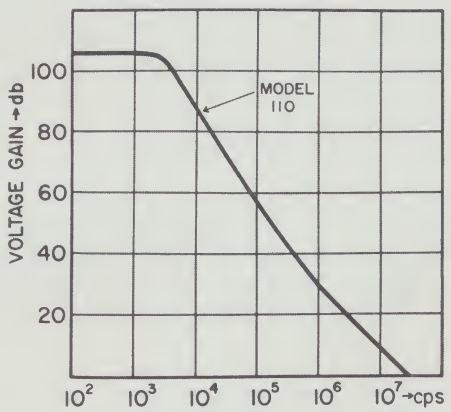
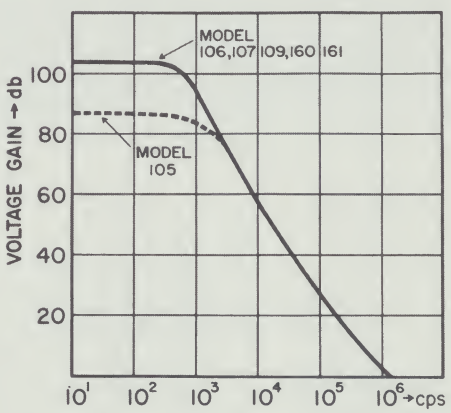


FIGURE 3
Mating socket AC1001

OPEN LOOP FREQUENCY RESPONSE







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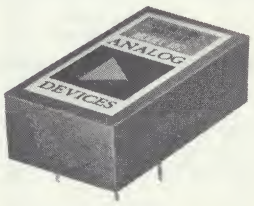
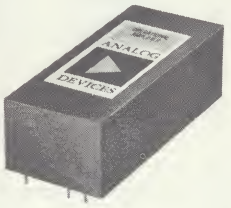
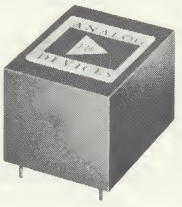
Fast Response Differential Inverting and NonInverting		*MODEL 102 — 10MC AND 30V/USEC* Gain — 10^6; Voltage Drift — 5uV/°C; Current Drift — 0.4/°C; Output — ±11V @ 20 ma; Input Impedance — 500 MΩ, CM; Full Output Response — 300KC
Ultra Low Voltage Drift Chopper Stabilized		*MODEL 202 — 0.2uV/°C* Current Drift — 0.5pa/°C; Gain — 10^9; Bandwidth — 10mc; Overload Recovery — 0.5usec; Output ±11V @ 20ma; Slew Rate — 30V/usec; Internal Chopper Drive
Ultra Low Input Current with High Input Impedance		*MODEL 301 — 1PA AND 10^{12} OHMS* Current Drift — 0.06pa/C; Noise — 1uV and 0.01pa; Voltage Drift — 30uV/°C; Gain — 10^6; Output — ±10V @ 20ma; Common Mode Voltage — ±300V
Low Cost — Fast Slew Rate Chopper Stabilized		*MODEL 210 — $157. AND 100V/USEC* Voltage Drift — 1uV/°C; Current Drift — 2pa/°C; Bandwidth — 20mc; Voltage Noise — 3uV; Output — ±10V @ 20ma; Overload Recovery — 0.2usec; Internal Chopper Drive
High Output Current		*MODEL 116 — ±11V AND 100MA.* Bandwidth — 10mc; Full Output Response — 500KC; Gain — 10^5; Noise — 3uV; Slew Rate — 30V/usec; Overload Recovery — 0.2usec; Fast Response on Non-Invertor

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Advantages of 12 db/Octave Operational Amplifiers and Their Application

Staff of Analog Devices, Inc.

In the design of operational amplifiers, primary emphasis has heretofore been given to making amplifiers which are simple to stabilize with large amounts of negative feedback. The fact that operational amplifiers having an open loop response with roll off faster than 6 db/octave offer substantial circuit design advantages over conventional 6 db/octave amplifiers has been largely overlooked. While it is true that fast roll off amplifiers are more difficult to stabilize, once the techniques for applying 12 db/octave amplifiers are understood, it is just as easy to use a 12 db/octave as a 6 db/octave amplifier and the high frequency performance is considerably improved. We shall discuss here the advantages of fast roll off operational amplifiers and the techniques for applying them.

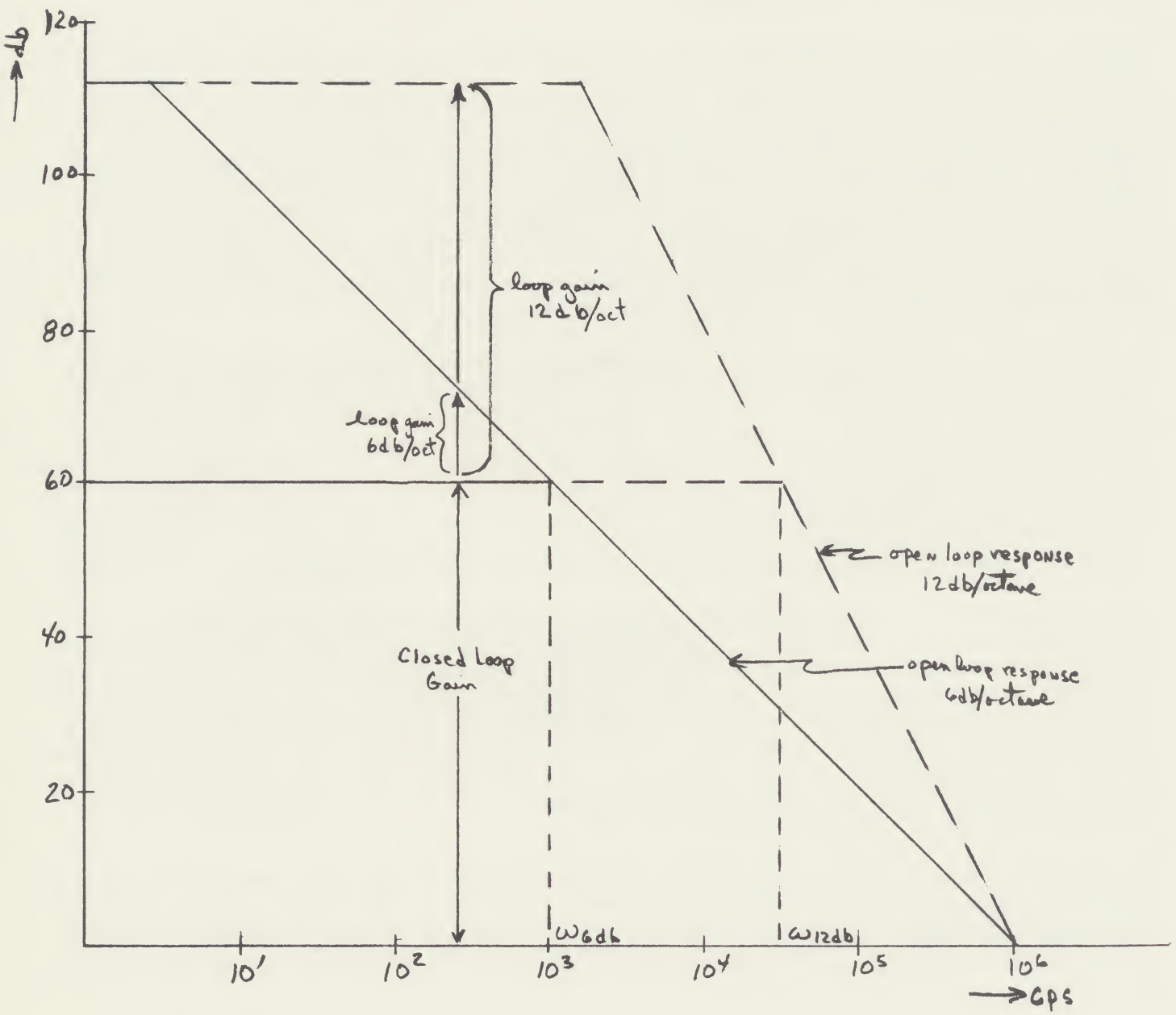
Figure 1 shows a comparison of open loop frequency response of a fast roll off amplifier and a conventional 6 db/octave amplifier. It is apparent that much higher closed loop bandwidth is possible with the 12 db/octave slope. For example, the bandwidth at a closed loop gain of 1000 is 30 KC as compared to 1 KC for a 6 db/octave amplifier. The virtues resulting from negative feedback; namely, high gain stability, low distortion, low output impedance and in some configurations, high input impedance, are all directly proportional to the amount of loop gain achieved at the frequency of interest. Another important advantage of the 12 db/octave amplifier is that loop gain at higher frequencies is considerably increased. Loop gain is the ratio of open loop to closed loop gain which appears on the log plot in Figure 1 as the difference in open and closed loop gains.

Another less obvious advantage to 12 db compensation is that the internal networks used to determine the open loop response of the amplifier permit full power output to much higher frequencies resulting among other things in faster slewing rates. Moreover, this design does not suffer the long delay in recovering from overloads which are inherent in 6 db/octave amplifiers. Broadband input noise also tends to be less since less high frequency attenuation occurs after the first stage, and noise due to the second and subsequent stages remains negligible at high frequencies compared with that of the input stage. The 6 db/octave roll off network causes so much attenuation that noise is increased due to contributions from the second and later stages.

An example of a 12 db/octave dc operational amplifiers is the Analog Devices, Inc., Model 101, shown in Figure 2. This amplifier, a general purpose differential input type, has a maximum voltage drift of 20 uV/°C and a maximum input current of 2 na, together with an output capability of ±11 V from dc to 30 KC. The transistor operating points and circuitry that produce this low drift and input current tend to produce low bandwidth. With the stabilizing networks used, however, the unity gain frequency in the inverting mode is 10 mc minimum while the open loop gain at 10 KC is over 6000, corresponding to a gain bandwidth product of 60 million minimum. Figure 3 is the open loop response for the Model 101.

Compared with the basic dc amplifier circuit stabilized with conventional 6 db/octave networks, the gain is over 100 times greater at 10 KC. The maximum frequency for full output has been increased 30 times, and overload recovery is 1000 times faster, only 200 usec typical. The only compromises made in the design to achieve these

Figure 1. Comparison of 12 db/octave and 6 db/octave Open Loop Response



results were a somewhat unsymmetrical input impedance--there is a capacitive load of 330 pf in series with 20 k from the negative input to ground--and the common mode voltage handling capability of ±10 V is reduced above 500 cps. The maximum common mode voltage limit determines the maximum high frequency output in the non-inverting mode. At unity gain full output of ±11 V is attainable to 500 cps. However, at a gain of 10 full output is attainable to 5 KC, and at a gain of 100 full output is attainable to 30 KC.

Techniques for Applying 12 db/Octave Amplifiers

The techniques for stabilizing a 12 db/octave amplifier will now be discussed. The open loop response given in Figure 3 shall be referred to in this discussion. However, the ideas present are applicable to any fast roll off amplifier.

Maintaining stable performance in feedback amplifiers is generally not enough. Good transient response is also required--usually no more than 10% overshoot for a step input and no ringing. Here are some types of feedback networks that will produce this good transient response with a fast roll off amplifier.

Capacitor Across Feedback Resistor

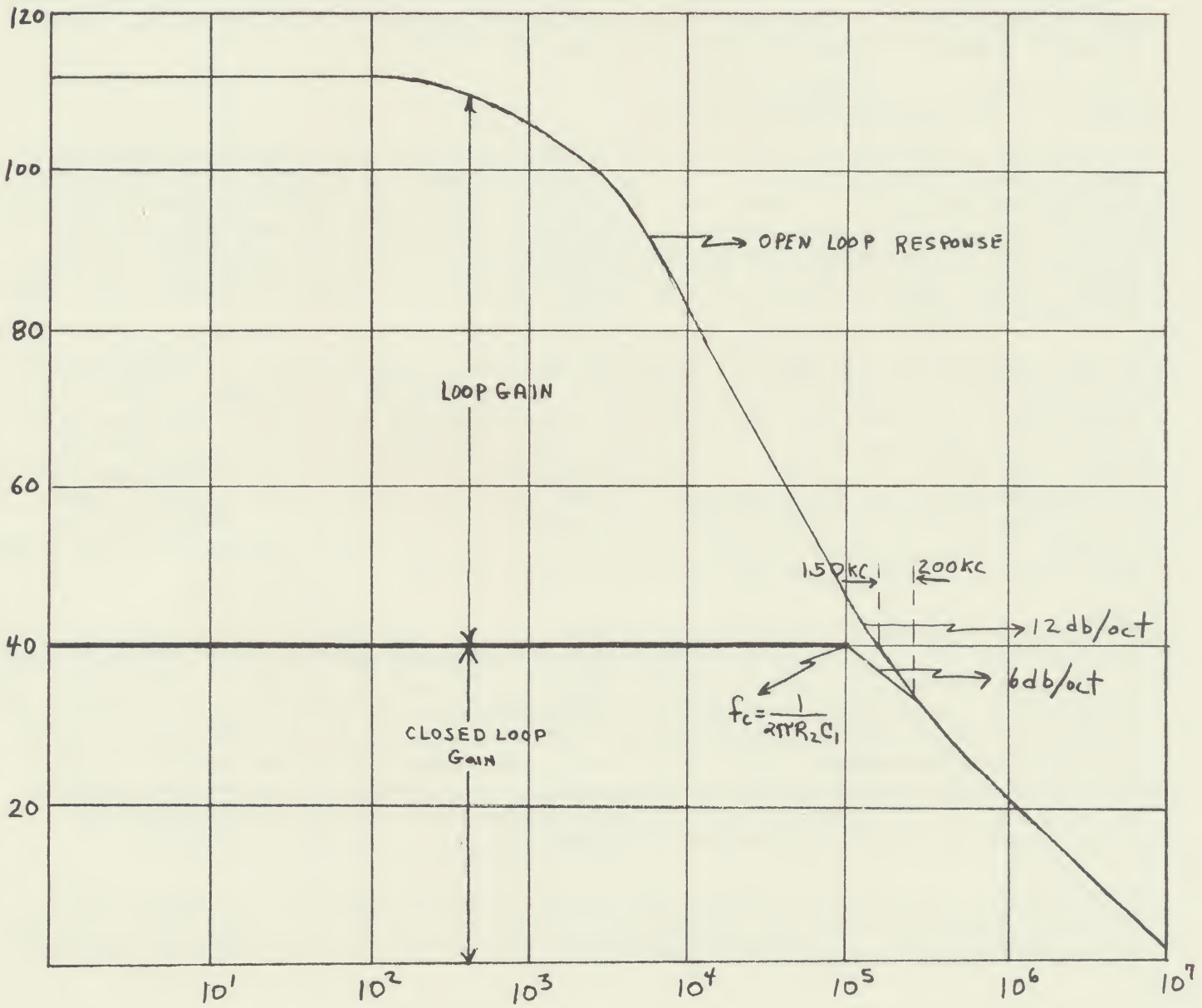
Assume the amplifier is to be used with a feedback network providing a closed loop gain of 100 or 40 db. For the inverting mode, as shown in Figure 4, the feedback network consisting of two resistors, R1 and R2, where R2 = 100 R1, determines the closed loop gain. Because of the very high open loop gain, 200,000 typical at dc, the negative or inverting input terminal is practically at ground potential. All the output voltage appears across R2 and all the input voltage appears across R1; so the gain is just R2/R1.

At high frequencies the gain is determined not only by the resistors but also by the open loop characteristics of the amplifier. It can be seen from Figure 3 that a resistive divider would cause the loop gain to pass through unity at 150 KC where the slope of the open loop gain curve is only a little less than 12 db/octave. Since the phase shift around the loop is roughly proportional to the slope of the response curve taken around the loop which amounts to 180° at 12 db/octave slope, it can be expected that a resistive divider will cause considerable ringing on a step input. In addition, if the impedance of the network is so high that input capacitance of the amplifier causes further phase lag, oscillation may result.

This problem is easily solved by connecting a small capacitor C1 across the feedback resistor R2. The capacitor provides a phase lead in the feedback path and increases the feedback above $f_c = 1/2\pi R2C1$, which is adjusted to 100 KC for this case. The net result is an increase in feedback so that unity gain around the loop now occurs at 200 KC on a slope of 6 db/octave instead of 12 db/octave. Phase shift at 200 KC is reduced to approximately 120°. Because there is only 9 db of loop gain at 100 KC, the closed loop response of the system is determined primarily by the r-c feedback network and is little affected by variations in the open loop gain of the amplifier which may occur due to tolerances in amplifiers or temperature variations.

Empirically, the optimum value of C1 for any closed loop gain and feedback resistance can be readily selected by feeding a square wave into the closed loop amplifier circuit and adjusting a variable capacitor to produce the desired transient response.

Figure 3. Open Loop Response With Compensation



This technique will result in the greatest bandwidth.

Table 1 presents a tabulation of values which have been found to give good transient response for various closed loop gains and impedance levels. The table also indicates the bandwidths which can be achieved by this design. In general, a value of 15 pf for C1 has been found satisfactory for a wide range of gain and impedance level over those shown in the table.

It is good practice to design an amplifier circuit for the minimum bandwidth permitted by the system requirements since wider band circuits are more susceptible to noise and stray coupling problems.

The use of a feedback capacitor works equally well for the non-inverting mode as shown in Figure 5. Since gain is this configuration is R1 + R2/R1 slightly different resistor values are needed for the same gain as the inverting mode. Moreover, for low gains, the optimum capacitor C1 is larger in the non-inverting mode because of loading across R1 due to the 330 pf input capacitance at the negative input previously mentioned.

High Source Impedance In Non-Inverting Configuration

There is always some stray coupling from the amplifier output to the non-inverting input. Feedback through the stray capacitance, Cs, is regenerative and may cause oscillations particula rly when a high source impedance is used. This problem can be remedied by a bypass capacitor, C2, as shown in Figure 6. The value for C2 must be greater than the closed loop gain times the stray capacitance, Cs. At very high gains the value for C2 may become quite large. For example, at closed loop gain of 10,000 and with stray coupling of only 1 pf, a capacitance of at least 0.02 uf would be required.

It is obviously desirable to minimize the stray capacitance in order to obtain good high frequency performance. Therefore, when laying out the circuit on a printed circuit board or other mounted socket, it is recommended the shielding consisting of B^+ , B^- or ground be interposed between the amplifier output and the non-inverting input which tends to reduce stray coupling. Stray capacitance within the amplifier itself is in the vicinity of 0.1 pf.

Handling Capacitive Loads

Connecting a large capacitive load across the output terminals can sometimes cause ringing or oscillations, particularly at low closed loop gains where the high frequency feedback is a maximum. Isolating the capacitive load by a 91 ohm resistor R4, as shown in Figure 7, completely eliminates this problem for any value of load capacitance. In most instances the increase in closed loop output impedance to 91 ohms has negligible effect on the circuit. However, for load impedances up to 0.002 uf, the output impedance for this circuit can be reduced to a fraction of an ohm by shunting R4 with a 22 uh rf choke (L1).

When larger load capacitances must be driven and the output impedance must be small at low frequencies, the load can be isolated by the network shown in Figure 8. Here the load is isolated by a 91 ohm resistor R4, and high frequency feedback is taken directly through capacitor C1 while low frequency feedback passes from the output terminals through R2 to the input. Because the feedback is taken directly from the output terminal, the output impedance can be in the milliohms at dc and low frequencies. Excellent transient response is attained with this circuit with load capacitances up to 0.01 uf. Higher or lower values of load capacitances can be driven

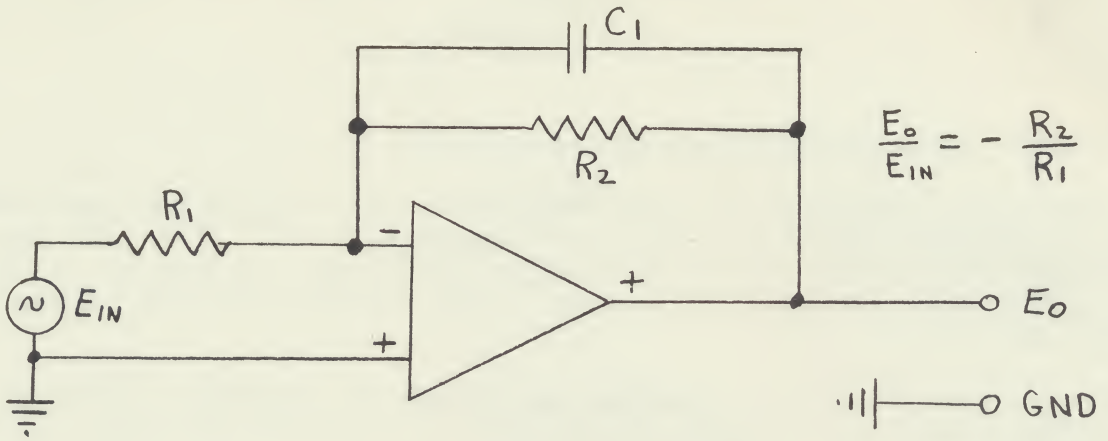


Figure 4. Use of High Frequency Feedback Capacitors

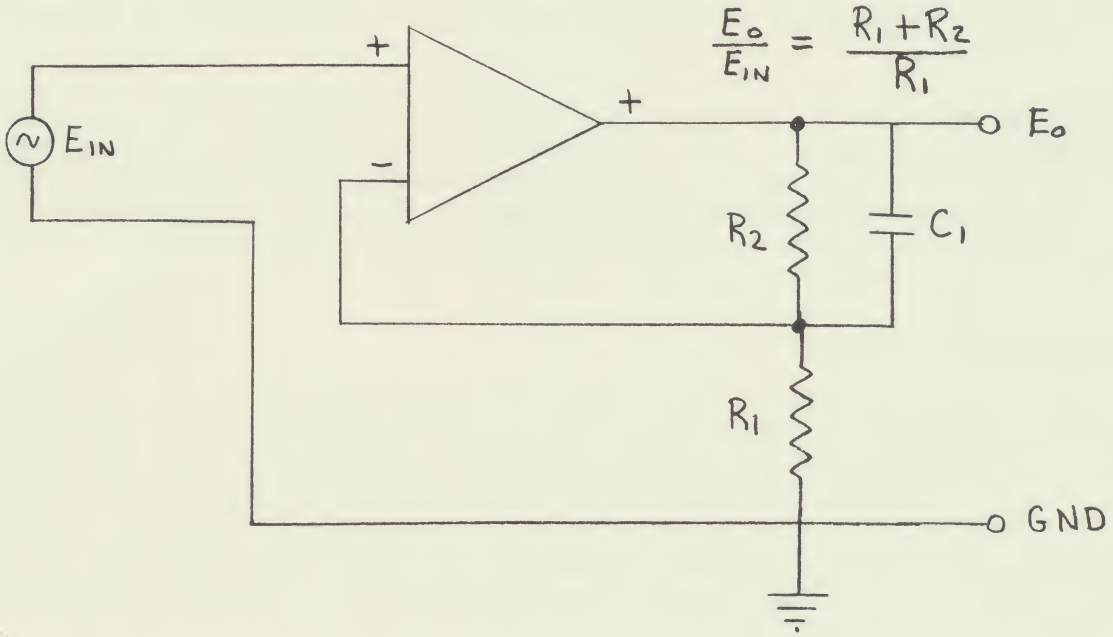


Figure 5. Non-Inverting Amplifier With High Frequency Feedback Capacitors

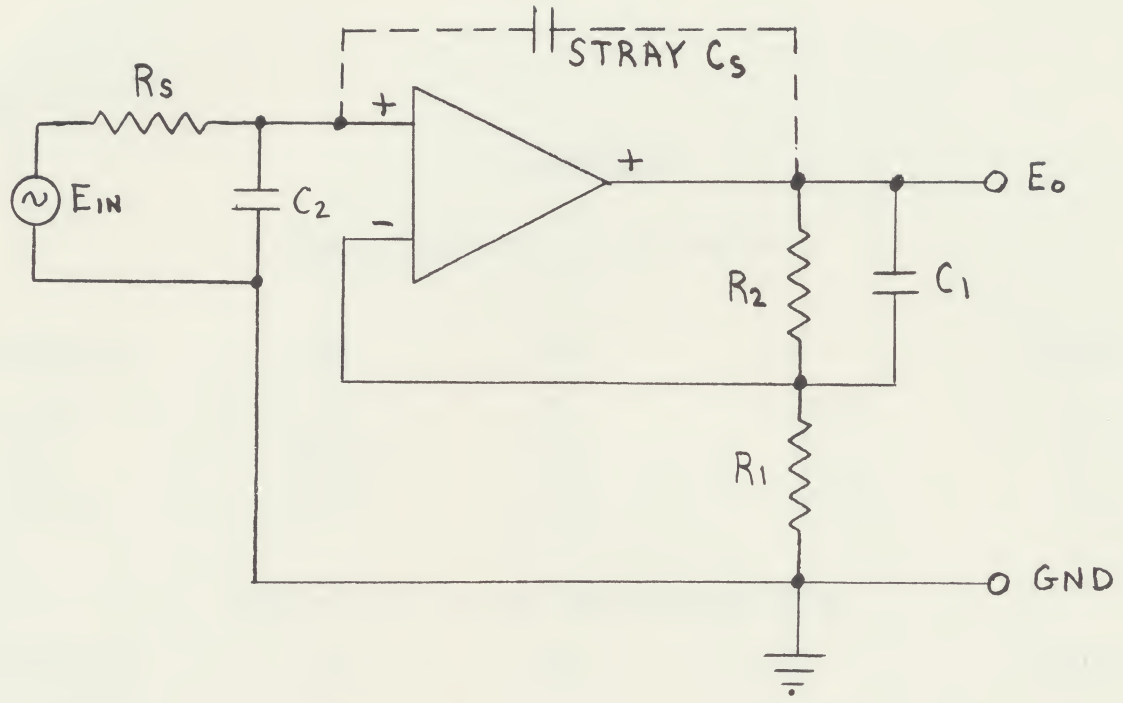


Figure 6. Non-Inverting Amplifier With Input Bypass Capacitor for High Source Impedance.

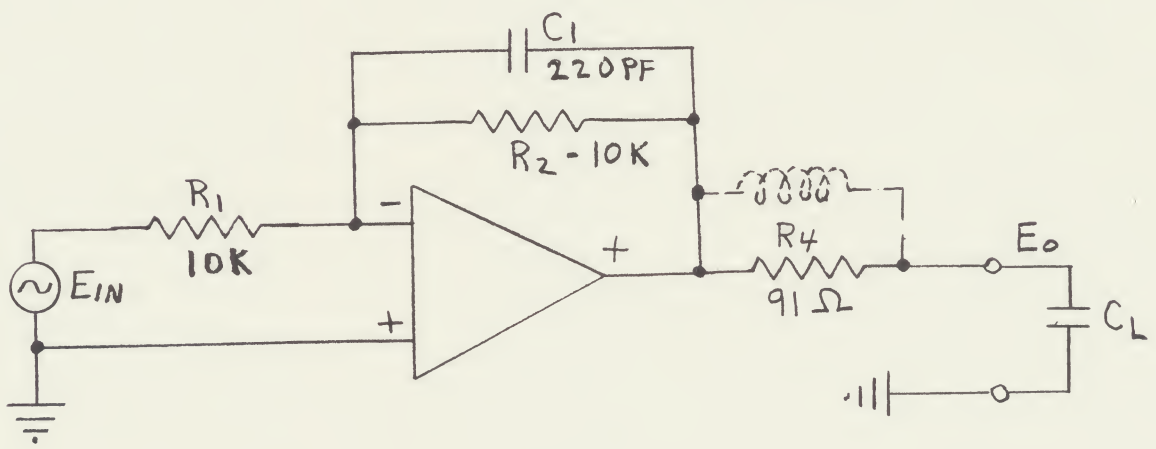


Figure 7. Capacitive Load Isolation

TABLE I

INVERTING MODE NETWORKS

GAIN	R1	R2	C1	BANDWIDTH
0	Infinite	0	0	15 mc
1	2 k	2 k	15 pf	5 mc
1	10 k	10 k	15 pf	1 mc
10	3.3 k	33 k	15 pf	350 kc

NON-INVERTING MODE NETWORKS

GAIN	R1	R2	C1	BANDWIDTH
1	Infinite	0	0	600 kc
10	1 k	9 k	100 pf	270 kc

NETWORKS FOR INVERTING OR NON-INVERTING MODE

GAIN	R1	R2	C1	BANDWIDTH
100	1 k	100 k	15 pf	120 kc
1,000	330	330 k	15 pf	35 kc
10,000	100	1 m	15 pf	6 kc

with good transient response by changing the value of C1 or C1 and R2. The circuit is basically a low-Q bridged-T network. Of course, the same arrangement can be used in the non-inverting mode.

Cable Capacitance in Remote Connections of Feedback Elements

Frequently an operational amplifier has to be wired to networks which may be located on switches or controls some distance away from the amplifier. Indiscriminate use of shielded wiring to these controls generally causes the feedback system to oscillate when a wideband operational amplifier is used. The problem can be easily handled by the addition of three components, C1, R4 and R5 in Figure 9. These components provide local feedback at high frequencies with short lead lengths that serves to reduce the high frequency gain around the external feedback path through R2. Resistor R5 and C1 limit the gain to unity at 1 mc, and since these components form an integrator, the gain from the junction of R1 and R2 falls off at only 6 db/octave instead of 12 db/octave. The output resistor R4 isolates capacitive loads and the loading of the shielded wiring. Practically any network can be used for R1 and R2. The closed loop bandwidth is limited by capacitor C1. This circuit, Figure 9, produces good transient response when using 10 feet of 91 ohm coaxial cable at the input and 10 feet at the output.

Differentiator

The differentiator, Figure 10, is just another case of isolating capacitive loading, this time at the input. Resistor R1 isolates the loading effect of C3 at high frequencies and limits the high frequency gain. The feedback capacitor, C1, 150 pf, provides the necessary phase lead at 100 KC and above to maintain excellent stability. Any desired value can be used for capacitor C3. With 0.01 uf the differentiator has a time constant of 100 usec.

As in all the previous circuits, it can be seen that the main principle involved is to provide a direct high frequency feedback path from the output to the inverting input that is isolated from capacitive loading at the extreme high frequencies.

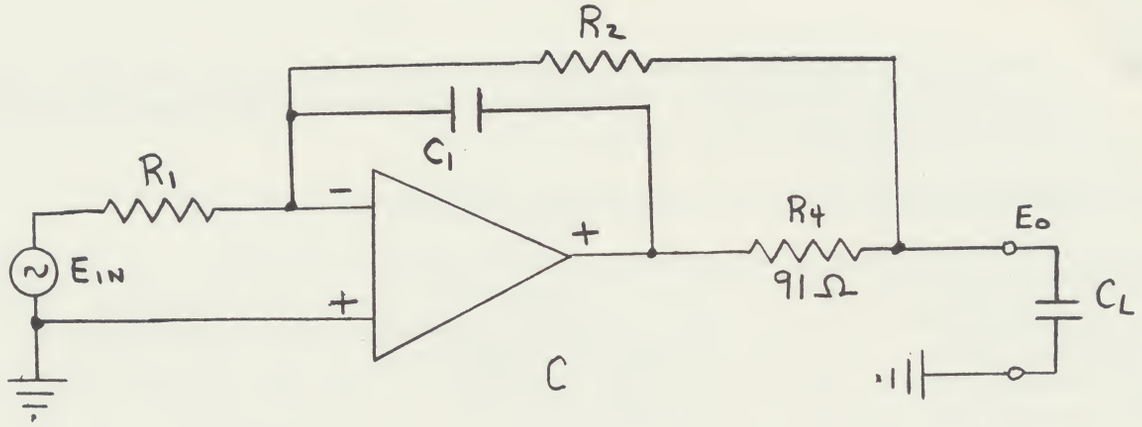


Figure 8. Capacitor Load Isolation With Low DC Output Impedance

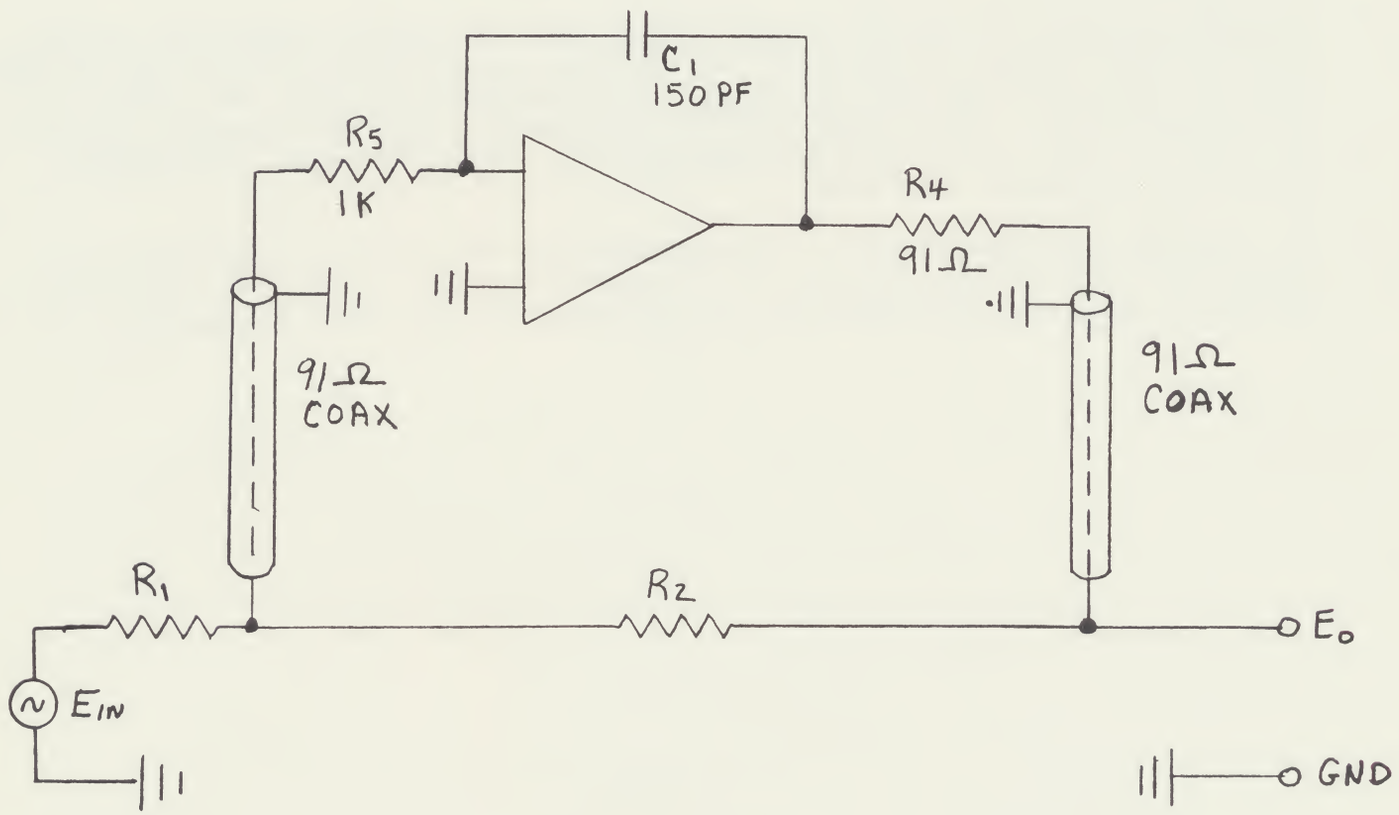


Figure 9. Feedback Network Remotely Connected With Capacitive Cable

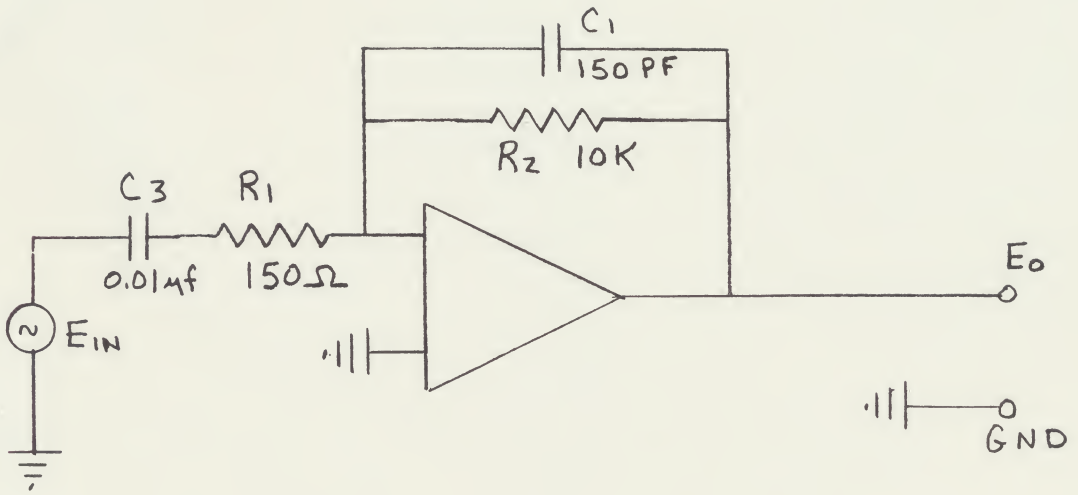


Figure 10. Differentiator

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PART IV — Offset and drift in operational amplifiers.

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ADVANTAGES OF 12 DB/OCTAVE OPERATIONAL AMPLIFIERS AND THEIR APPLICATION

OPERATIONAL AMPLIFIERS, PART IV

Offset and drift in operational amplifiers

Ray Stata, Vice President
Analog Devices, Inc., Cambridge, Mass.

In our previous articles, Operational Amplifiers — Parts I and II it was erroneously stated that the effect of voltage source drift and noise is increased when the summing or source impedance exceeds the open loop input impedance of an operational amplifier. This depends on the equivalent circuit which applies to the published specifications. In this article the correct equivalent circuit is given for the offset parameters and it is shown that closed loop drift performance is completely independent of the value for open loop input impedance regardless of the relative values for the summing and feedback impedance in any amplifier configuration. We regret our previous error and we hope this article will clarify any confusion on this subject.

INTRODUCTION

One of the most fundamental limitations of DC amplifiers, including operational amplifiers, is offset drift. This article will discuss the precise meaning of open loop offset specifications as given by operational amplifier manufacturers and will give equivalent circuits which can be used to predict closed loop offset behavior.

An ideal operational amplifier would have exactly zero output for zero input. This is never quite the case in practice where an amplifier will exhibit some output for zero input signal. The output may include random and spurious AC signals which are generally called noise and a DC signal which is called offset. It is customary in specifying these signals to refer them to the input so that they are then independent of the amplifier's gain. Input offset is then defined as the input required to zero the DC component of the output with zero input signal.

A fixed input offset is usually not a problem since biasing circuits can be devised to cancel this signal. However, changes in input offset due to variations of ambient temperature, supply voltage and component values with time introduces a basic measuring error, since these offset changes cannot be distinguished from changes of input signal. It is customary to refer to changes of offset as "drift". Remember that drift differs from offset in that drift relates the coefficient of offset change either in uV/°C or, uV/day or uV/V; whereas offset refers to the magnitude of voltage (or current as the case may be) required to zero the output at a given temperature, time and supply voltage.

Actually, offset drift can be considered another form of noise which occurs at very low frequencies. Although this article will be primarily confined to a discussion of offset and drift, the equivalent circuits given and many of the conclusions drawn apply to higher frequency noise as well.

EQUIVALENT CIRCUIT FOR OFFSET OF SINGLE-ENDED AMPLIFIER

Figure 1 shows an equivalent circuit which can be used to explain the offset behavior of a single-ended operational amplifier. Remember that an equivalent circuit is only a model and the test of its validity is, 1) does it explain the observed performance of the amplifier and 2) do the coefficients used in the model correspond to those which are measured and published for the amplifier. From empirical observations it is found that for relatively low values of circuit impedances in the external feedback networks the magnitude of input offset is almost independent of the impedances used. However, for large values of feedback impedances, input offset increases almost proportional to the magnitude of the impedances used. To explain this effect it is necessary to include both an offset voltage and offset current source in the equivalent circuit as shown in Figure 1.

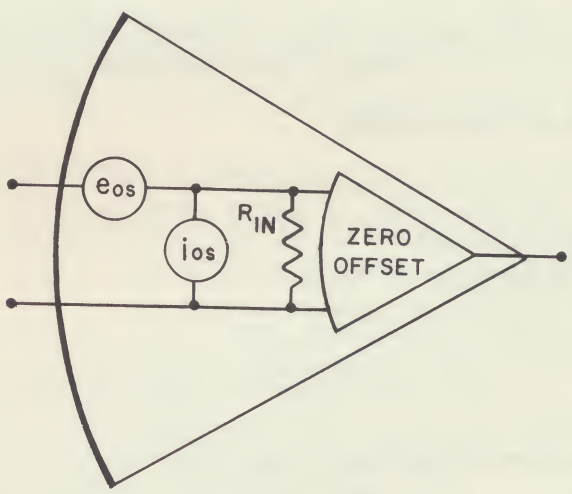

Fig. 1 — Equivalent Circuit For Single-Ended Amplifier

The voltage offset source, e_{os}, is defined as the voltage required at the input to zero the amplifier output assuming zero source impedance. The current offset source, i_{os}, is defined as the current required

at the input to zero the output assuming infinite source impedance. R_{IN} represents the open loop input impedance (between inputs) measured under null conditions, that is, very small input signals. The amplifier following the equivalent input circuit would be ideal to the extent of having zero offset and infinite input impedance, but it would have finite gain and bandwidth.

The primary factors contributing to offset voltage may be expressed by the following equation:

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T}\Delta T^{+} \frac{\Delta e_{os}}{\Delta V^{+}}\Delta V^{+} + \frac{\Delta e_{os}}{\Delta V^{-}}\Delta V^{-} + \frac{\Delta e_{os}}{\Delta t}\Delta t$$

where,

1. E_{os} is the initial offset voltage usually measured at 25° C ambient with nominal power supply voltages.
2. $\Delta e_{os}/\Delta T$ is the temperature drift coefficient usually given in uV /° C averaged over some specified temperature range.
3. $\Delta e_{os}/\Delta V^{+}$ and $\Delta e_{os}/\Delta V^{-}$ are the supply voltage drift coefficients for both positive and negative supplies. Normally only one value is given, either in uV/% or uV/V, for whichever coefficient is larger and assuming that only one supply voltage is changed at a time. For most operational amplifiers the positive coefficient is considerably greater and hence is the value specified.
4. $\Delta e_{os}/\Delta t$ is the drift coefficient vs. time usually given in uV/day.

Likewise, the primary factors contributing to offset current may be expressed by the following equation:

$$i_{os} = I_{os} + \frac{\Delta i_{os}}{\Delta T}\Delta T + \frac{\Delta i_{os}}{\Delta V^{+}}\Delta V^{+} + \frac{\Delta i_{os}}{\Delta V^{-}}\Delta V^{-} + \frac{\Delta i_{os}}{\Delta t}\Delta t$$

where the current offset coefficients are defined similarly to the voltage offset coefficients above.

CLOSED LOOP OFFSET BEHAVIOR

The preceding equivalent circuit and definitions may now be applied to predict offset behavior in a closed loop circuit. Let us take as an example the simple inverting amplifier in Figure 2.

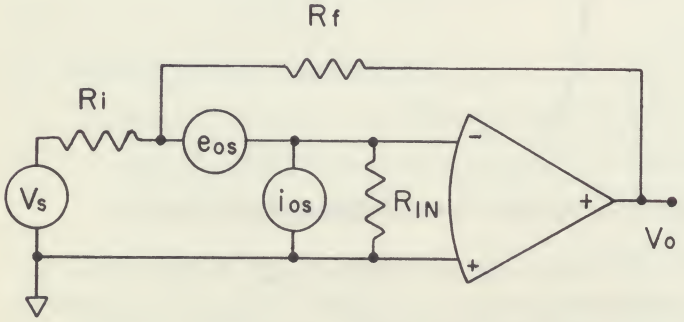

Fig. 2 — Simple Inverting Amplifier

In this circuit it is most revealing to refer the voltage and current offset errors to the source voltage, V_s, as shown in Figure 3.

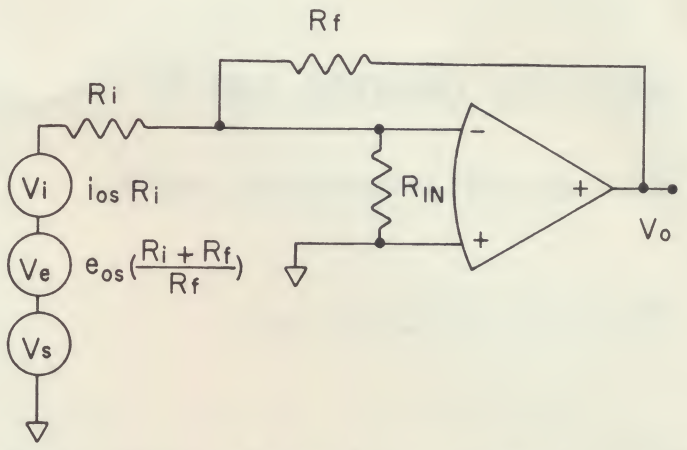

Fig. 3 — Offset Errors Referred To Source Voltage

Total error due to offset referred to the source voltage is then,

$$\Delta V_s = i_{os}R_i + e_{os}\frac{R_i + R_f}{R_f}$$

Offset can be referred to the output by multiplying by closed loop gain as follows:

$$V_o = \left[-\frac{R_f}{R_i}V_s - i_{os}R_f - e_{os}\frac{R_i+R_f}{R_i}\right]\left[\frac{1}{1+\frac{1}{A}\left(1+\frac{R_f}{R_i \,||\, R_{IN}}\right)}\right]$$

where A is open loop voltage gain.

Several important conclusions can be drawn from the above analysis:

1. Finite open loop input impedance, R_{IN}, has absolutely no effect on voltage and current offset referred to the source voltage regardless of how large R_i and R_f may be compared to R_{IN}. Referred to the output R_{IN} has only a second order effect inasmuch as it contribures to gain error, but the signal to noise ratio at the output is uneffected by R_{IN} since both signal and offset error are multiplied by the same gain error.

2. Voltage offset referred to the source voltage is multiplied by the factor $(R_i+R_f)/R_f$ to account for the voltage division between R_i and R_f. Thus for low values of closed loop gain (R_f/R_i) the effect of voltage offset is increased by as much as a factor of two at unity closed loop gain.

3. The effect of current offset referred to the source voltage can be obtained by assuming all of the offset current is supplied by the source voltage generating a voltage drop $i_{os}R_i$. Actually offset current is supplied both from the output and the source voltage in ratios depending on R_i and R_f. But the portion supplied by the output must be divided by closed loop gain to be referred to the input, which yields the same result as if all offset current were supplied by the input.

$$V_i = i_{os}\frac{R_f}{R_i+R_f}R_i + i_{os}\frac{R_i}{R_i+R_f}R_f\frac{R_i}{R_f} = i_{os}R_i$$

supplied by input — supplied by output

4. The relative importance of voltage and current offset depends on the magnitude of R_i. Considering offset drift due to temperature only, the temperature coefficent referred to the source voltage would be,

$$\frac{\Delta V_s}{\Delta T} = \frac{\Delta e_{os}}{\Delta T}\frac{R_i + R_f}{R_f} + \frac{\Delta i_{os}}{\Delta T}R_i$$

If we take the example of an amplifier with drift coefficients of 20uV/°C and 1na/°C, we can construct the table in Figure 4 showing input drift $\Delta V_s/\Delta T$ versus input impedance, R_i. (Assuming $R_f >> R_i$.)

R_i	$\Delta e_{os}/\Delta T$	$R_i\Delta i_{os}/\Delta T$	$\Delta V_s/\Delta T$
1K	20uV/°C	1uV/°C	21uV/°C
2K	20uV/°C	2uV/°C	22uV/°C
5K	20uV/°C	5uV/°C	25uV/°C
10K	20uV/°C	10uV/°C	30uV/°C
20K	20uV/°C	20uV/°C	40uV/°C
50K	20uV/°C	50uV/°C	70uV/°C
100K	20uV/°C	100uV/°C	120uV/°C

Fig. 4 — Drift vs. Input Impedance

Note that for R_i=20K ohms, the contributions due to voltage drift and current drift are equal. For R_i < 20 K ohms, drift performance is due primarily to voltage drift, being nearly independent of the value for R_i. For R_i>20K ohms, drift is due primarily to current drift, increasing almost proportional to R_i.

Since the closed loop input impedance of the inverting amplifier is equal to R_i, we see that large input impedance can be obtained only at the expense of offset errors for

$$R_i > \frac{\Delta e_{os}}{\Delta T} \Big/ \frac{\Delta i_{os}}{\Delta T}$$

Example: Let us illustrate these results by a sample calculation of offset errors for the inverting amplifier in Figure 2.

Problem: Input Voltage (V_s) = 500mV, closed loop gain (R_f/R_i) = 10, input impedance = 50K ohms. Calculate maximum input offset errors for a temperature range of 0 to 50°C and for supply voltage regulation of 0.5% over a period of one day. Assume that initial input offset is adjusted to zero at 25°C and that the operational amplifier has the following drift coefficients:

$$\frac{\Delta e_{os}}{\Delta T} = \pm 20uV/°C \qquad \frac{\Delta i_{os}}{\Delta T} = \pm 1na/°C$$

$$\frac{\Delta e_{os}}{\Delta V^+} = \pm 20uV/\% \qquad \frac{\Delta i_{os}}{\Delta V^+} = \pm 2na/\%$$

$$\frac{\Delta e_{os}}{\Delta t} = \pm 50uV/day \qquad \frac{\Delta i_{os}}{\Delta t} = \pm 5na/day$$

Solution: R_i = 50K ohms, R_f = 500K ohms

$$e_{os} = \pm\left(\frac{20uV}{°C}\right)25°C \pm \left(\frac{20uV}{\%}\right).5\% \pm \left(\frac{50uV}{day}\right)(1day) = \pm 560uV$$

$$i_{os} = \pm\left(\frac{1na}{°C}\right)25°C \pm \left(\frac{2na}{\%}\right).5\% \pm \left(\frac{5na}{day}\right)(1day) = \pm 31na$$

Input Offset Error

$$\Delta V_s = e_{os}\frac{R_f + R_i}{R_i} + R_i I_{os} = \pm 2.2mV$$

$$\% \text{ error} = \frac{\Delta V_s}{V_s} = 0.44\%$$

NON-INVERTING AMPLIFIER

The offset behavior of the non-inverting amplifier can be predicted by the circuit in Figure 5 where again the voltage and current offset are referred to the source voltage. R_s is the source impedance.

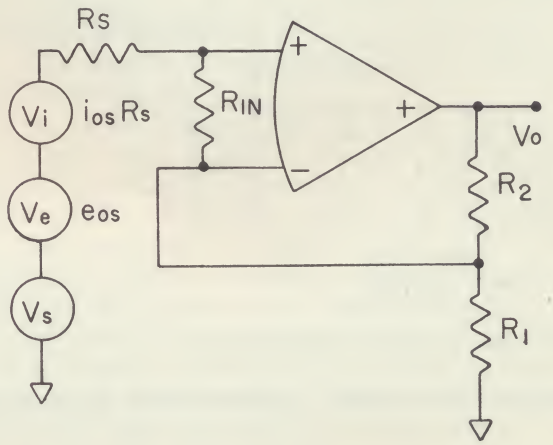

Fig. 5 — Non-Inverting Amplifier

For this circuit the following points should be noted:

1. Unlike the inverting amplifier, voltage offset referred to the source voltage is independent of closed loop gain. Thus, there is no increase in voltage drift (and noise) at unity or low values of closed loop gain.
2. As for the inverting amplifier, voltage and current offset referred to the source voltage is completely unaffected by the value for R_{IN}.
3. The effect of current offset referred to the source voltage is directly proportional to the source impedance, R_s. (In parallel with any other impedances to ground such as biasing networks.)
4. Unlike the inverting amplifier, very large input impedance can be obtained without increasing offset errors.

CURRENT TO VOLTAGE AMPLIFIERS

Many devices such as photocells and photomultipliers produce an output current from a relatively high source impedance. These devices can best be characterized by a current source as shown in Figure 6. In this circuit configuration the operational amplifier converts the input current to an output voltage with a low output impedance. Gain is proportional to R_f.

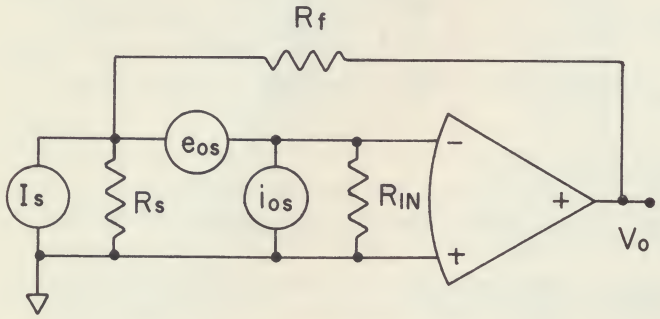

Fig. 6 — Current To Voltage Converter

In analyzing this circuit, it is more revealing to refer the voltage and current offsets to the signal source as current sources as shown in Figure 7.

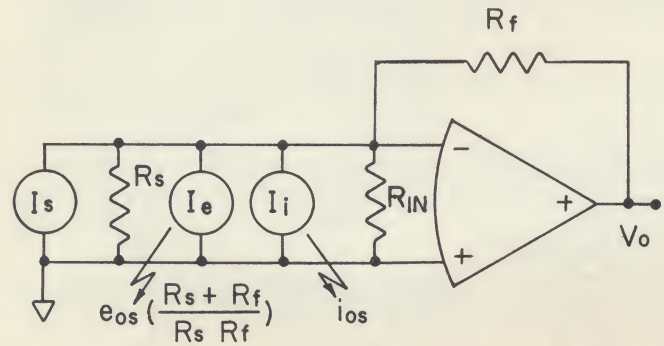

Fig. 7 — Offset Errors As Current Sources

Thus the offset errors referred to the signal source are:

$$\Delta I_s = e_{os}\frac{R_s + R_f}{R_s R_f} + i_{os}$$

To refer the signal and offset errors to the output we multiply by closed loop gain,

$$V_o = \left[-I_s R_f - e_{os}\frac{R_s+R_f}{R_s} - i_{os}R_f\right]\left[\frac{1}{1+\frac{1}{A}\left(1+\frac{R_f}{R_{IN}\,||\,R_s}\right)}\right]$$

From this analysis we can draw the following conclusions:

1. Open loop input impedance, R_{IN}, has no bearing on signal to offset ratio (or signal to noise ratio) referred to either the signal source or the output.
2. For $R_s \gg R_f$, which is generally the case for a high impedance current source, voltage offset (and noise) is not amplified referred to the output and therefore can often be ignored as compared to the effect of offset current.
3. Referred to the output, offset current like signal current is multiplied by R_f and the principle error is usually the ratio of offset current (and noise) to signal current.

EQUIVALENT CIRCUIT FOR DIFFERENTIAL INPUT AMPLIFIERS

Thus far, we have been discussing offset behavior for single - ended amplifiers. There are additional considerations for differential type amplifiers since each input has its own offset current source. Differential amplifiers depend on symmetry of the input circuitry for their proper operation and therefore it is reasonable to expect that the offset current at each input would be about equal and that changes in offset current would tend to track for changes in ambient temperature and supply voltage. This fact can be used to minimize input offset errors as we shall discuss.

Figure 8 shows the equivalent circuit for a differential amplifier.

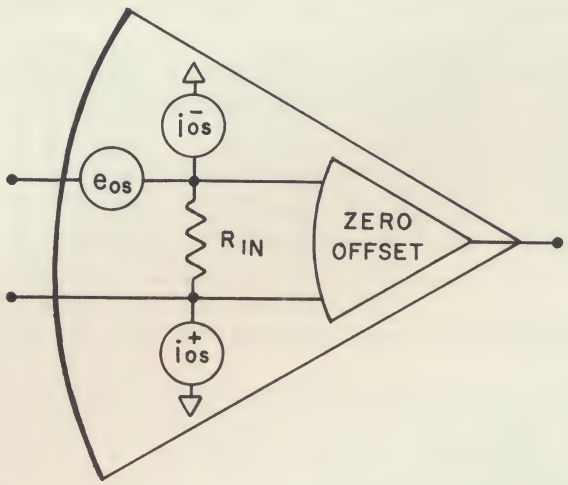

Fig. 8 — Equivalent Circuit For Differential Amplifier

We must now define another term, differential offset current, as follows:

$$i_{osd} = (i^-_{os} - i^+_{os}) = (I^-_{os} - I^+_{os}) + \frac{\Delta(i^-_{os} - i^+_{os})}{\Delta T}\Delta T + \text{etc.}$$

where

1. $(I^-_{os} - I^+_{os})$ is the initial difference in offset current at each input required to zero the output usually specified at 25° C with nominal supply voltage.
2. $\Delta(i^-_{os} - i^+_{os}) / \Delta T$ is the differential offset current temperature drift coefficient.

For transistor type differential amplifiers, offset current at each input as well as drift of offset current with temperature tends to track to within 20% to 30%. Or in other words, offset current at each input is about 3 to 5 times greater than the differential offset current. At this point, we should mention that there is great confusion between the definitions used

by discrete component manufacturers and integrated circuit manufacturers of operational amplifiers. Discrete component manufacturers such as Philbrick, Burr-Brown, Nexus and Analog Devices' use the definitions given here in specifying offset current.

Integrated circuit manufacturers define current at each input (i_{os}^- and i_{os}^+) as input bias current while they call differential input current ($i_{os}^- - i_{os}^+$) input offset current. Thus specifications for offset current and offset current drift can differ by 3 to 5 times depending on the definitions used.

Initial offset current also bears further discussion. It is possible to reduce initial offset current at a given temperature and supply voltage arbitrarily close to zero by using networks internal to the amplifier to supply a biasing or compensating current. This adjustment procedure will have no effect on the drift coefficients of offset current. In a few applications a very low value for initial offset current is a definite requirement. However, in most applications, initial offset current is of no consequence since it can be compensated for by external circuitry, in which case offset current drift is the only source of error.

CLOSED LOOP OFFSET PERFORMANCE OF DIFFERENTIAL INPUT AMPLIFIERS

Since offset current at each input tends to be equal, if we equalize the impedance of each input to ground, we tend to cancel the errors due to offset current. For example, the simple inverting amplifier is shown in Figure 9 with an offset current compensating resistor, R_C, in the non - inverting input. We have used the equivalent circuit of Figure 8 and have referred all of the offset errors to the source voltage. The by-pass capacitor, C, which is used to prevent loss of open loop gain at high frequencies, is optional.

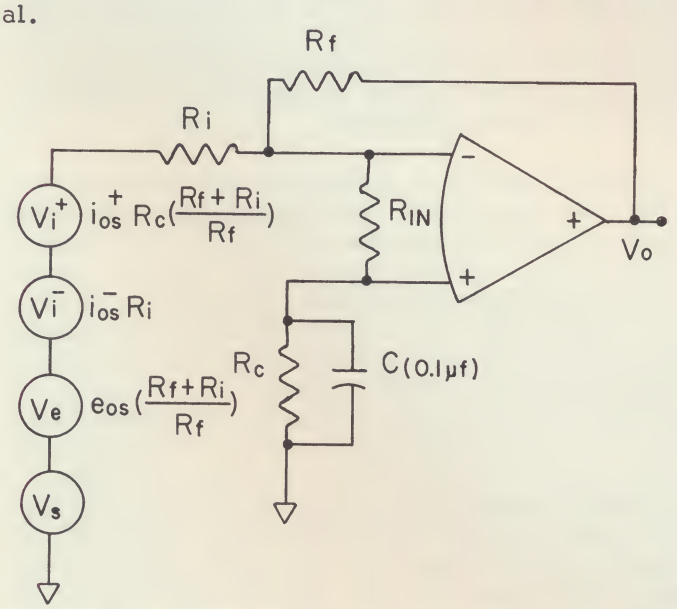

Fig. 9 — External Offset Current Compensation

If we set $R_C = R_i R_f / R_i + R_f$ then the total input offset error is,

$$\Delta V_S = e_{os} \frac{R_f + R_i}{R_f} + R_i (i_{os}^- - i_{os}^+)$$

Thus by equalizing the impedance at each input, offset behavior is then determined by differential offset current which is generally 3 to 5 times less than offset current.

INITIAL OFFSET ADJUSTMENTS

It is generally desirable or necessary to have some provisions for adjusting the initial input offset to zero. For the inverting amplifier, assuming $R_f >> R_i$, we know that initial offset errors referred to the source voltage are:

$$\Delta V_s = E_{os} + R_i I_{os} \quad \text{(for single-ended amplifier or with } R_c = o\text{)}$$

$$\Delta V_s = E_{os} + R_i (I_{os}^- - I_{os}^+) \quad \text{(for differential amplifier with } R_c = R_i \| R_f\text{)}$$

Most operational amplifiers have provisions for adding an external potentiometer to zero initial offset voltage, E_{os}. This adjustment will also zero errors due to initial offset current by unbalancing the input circuit of the amplifier to generate an equal and opposite voltage to compensate for ($R_i I_{os}$). However, it is bad practice to use the voltage offset potentiometer to balance the amplifier when the initial offset, ΔV_s, is predominately due to offset current (more precistely when $R_i I_{os}$ or $R_i (I_{os}^- - I_{os}^+)$ is greater than 4 - 5 millivolts). The reason is that a large unbalance of the input stage of the amplifier, which may be required to compensate for offset current, can degrade the temperature drift performance of the amplifier.

For the case where $I_{os} R_i$ or $(I_{os}^- - I_{os}^+) R_i >> E_{os}$ the voltage offset balance potentiometer should be replaced by a fixed resistor and an adjustable bias current should be summed as shown in Figure 10. Note that this current bias adjustment will zero both voltage and current offset for a fixed source impedance. For the exotic case where a precise input zero must be maintained under conditions of varying source impedance then both the current bias adjustment and the voltage offset potentiometer must be used to zero both E_{os} and I_{os} independently.

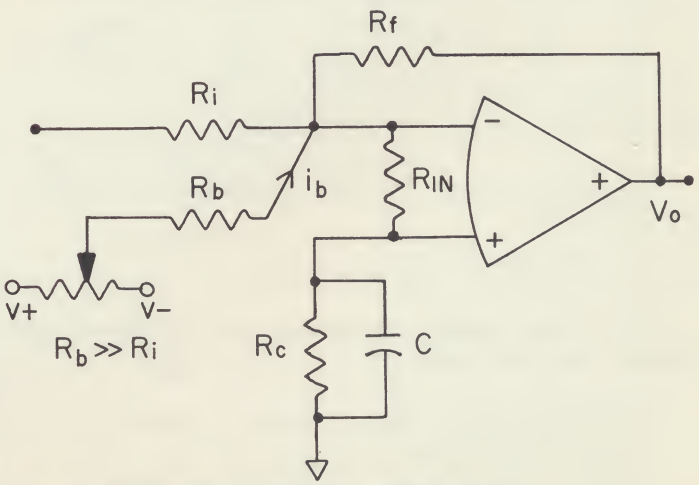

Fig. 10 — External Offset Current Bias Circuit

The non-inverting amplifier presents another problem when an external current bias circuit is used.

Usually the non-inverting amplifier is used to obtain very large input impedance. If we used the circuit in Figure 10 to supply offset current to the signal input we would lower the input impedance. A preferable circuit is shown in Figure 11 where the biasing network does not effect the input impedance.

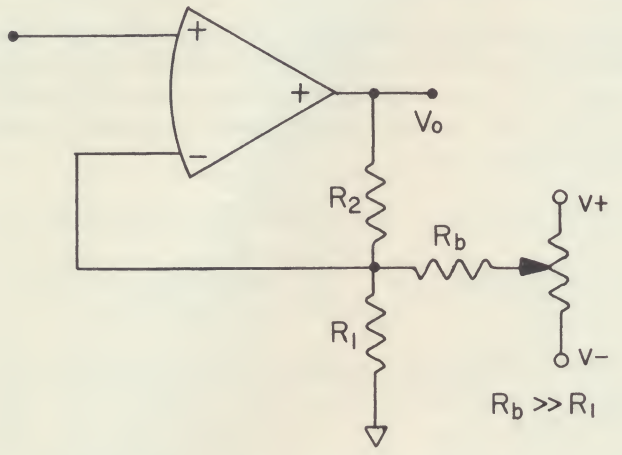

Fig. 11 — Bias Circuit For Non-Inverting Amplifier

TEST CIRCUIT FOR OFFSET VOLTAGE AND CURRENT

A convenient circuit for measuring offset parameters is shown in Figure 12.

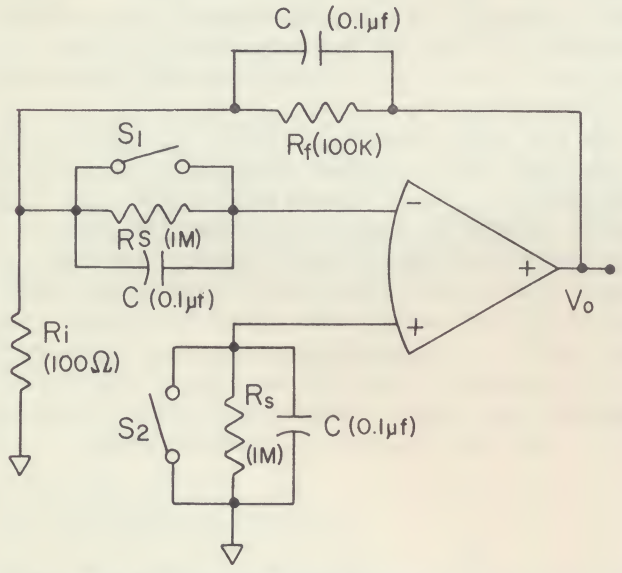

Fig. 12 — Test Circuit For Offset Parameters

The output voltage for this configuration, assuming $R_f \gg R_i$, is,

$$V_o = - R_f/R_i \, (e_{os} + i_{os}^- R_s - i_{os}^+ R_s)$$

The various offset parameters are measured as follows assuming that $R_s \gg e_{os} / (i_{os}^- - i_{os}^+)$:

1. Voltage Offset, e_{os}, - Close S_1 and S_2
   $V_o = - R_f/R_i \, e_{os}$
2. Offset Current, i_{os}^- - Close S_2, Open S_1
   $V_o = - R_f/R_i \, R_s \, i_{os}^-$
3. Offset Current, i_{os}^+ - Close S_1, Open S_2
   $V_o = - (R_f + R_i/R_i) R_s \, i_{os}^+ \approx R_f/R_i \, R_s \, i_{os}$
4. Differential Offset Current, $(i_{os}^- - i_{os}^+)$, - Open S_1 and S_2
   $V_o = - R_f/R_i \, R_s \, (i_{os}^- - i_{os}^+)$

The various offset coefficients are measured by varying a parameter such as temperature or supply voltage and recording the output voltage for the different switch positions.

OTHER DRIFT CONSIDERATIONS

Drift performance of differential operational amplifiers depends on the cancellation of temperature effects in matched components presumed to be at precisely the same temperature. Thermal gradients in the vicinity of the amplifier can cause input offsets an order of magnitude greater than predictable from the specifications. For example, a difference in temperature of only .01C between the junctions of two otherwise perfectly matched transistors in the input stage produces an input offset of 24uV. For this reason, over a narrow range of operating temperature, the input offset performance of differential amplifiers is more sensitive to thermal gradients than to actual change in ambient temperature. Over large changes of ambient temperature, thermal gradients are proportionately less significant in their effect on input offset although quite large offset transients can occur during large step changes in temperature due to non-uniform temperature rise. In critical applications in non-uniform temperature environments a shield or insulator should be used around differential amplifiers to create an isothermal surface.

One of the important but less obvious advantages of chopper stabilized operational amplifiers is that their drift performance does not depend on the cancellation of temperature effects in matched components and therefore offset performance is relatively immune to thermal gradients.

Another anamoly in specifying drift performance is that the temperature drift coefficients are generally specified as the average drift over a given temperature range. This is done for two reasons: first, a relatively large increment in temperature is required to eliminate the effects of thermal gradients from the measurements and secondly, it is not economical to record data and compute the drift coefficients for a large number of temperature increments. Figure 13 shows a typical graph of offset voltage vs. temperature as compared to the average drift coefficient. At the extremes of temperature the actual slope (uV/° C) may exceed the average slope, while in the vicinity of room temperature the actual slope may be less. It is also possible that the slope can be in either direction and in some cases the actual curve can slope up (or down) at both extremes of temperature.

Actually, a less misleading method of specifying offset performance would be to state the offset voltage change over a given temperature range.

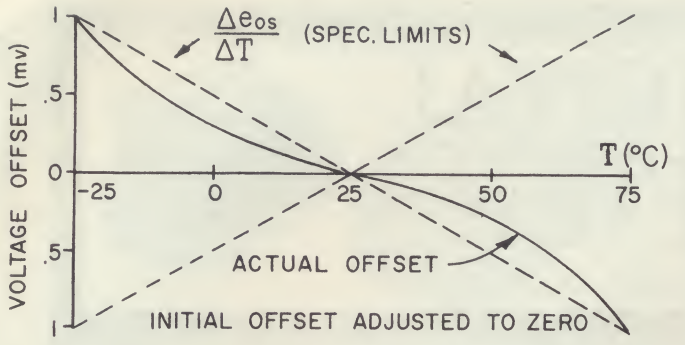

Fig. 13 — Voltage Offset vs. Temperature

Self-heating of the amplifier module following the application of power supply voltages can cause a change in initial offset voltage and current. The magnitude and duration of this warm up drift depends on the size and thermal mass of the module , the output voltage and current ratings and the arrangement of the components in the amplifier layout. In general this effect is more severe for large output voltage and current amplifiers which is one reason to consider the use of a separate booster amplifier so that the large temperature changes in the output stage are physically separated from the sensitive input transistors. Warm up offset voltage changes of 100 uV to 1 mV are possible over a time period of 15 to 20 minutes or longer.

Another source of input offset , which is sometimes overlooked , is due to rectification of high frequency overdrive signal. The specification for full output voltage or power response is usually regarded as a limitation on the output slewing rate capabilities of the amplifier. However, another reason for this specification is that input offsets can be generated when the the input signal contains frequency components which exceed the full output response specification. This accounts for the fact that the full output response capability of an amplifier can sometimes be less than that which can be predicted from the slewing rate specification.

TYPICAL DRIFT PERFORMANCE

At least four basic types of operational amplifiers are now commercially available to meet an extremely wide range of requirements for offset and drift performance. The table in Figure 14 gives some indication of the range of specifications which can be achieved with the various amplifier types.

Transistor Differential - The performance of transistor differential operational amplifiers is quite adequate for the vast majority of applications. Due to their relatively low cost and the versatility of the differential input design, these units are by far the most widely used. Since the offset current drift is relatively high, the impedance of the external input circuit should not be much greater than 100K ohms. Where long term offset stability over several months is important, metal film resistors should be used in the design of the input stage of the amplifier.

F.E.T. Differential - The primary advantage of FET amplifiers is their lower initial offset current and their lower offset current drift. This allows many megohms to be used in the external input circuit without excessive drift. Voltage offset drift, on the other hand, both with time and temperature is not so good for FET's as for transistors and these devices are more expensive.

Chopper Stabilized - Chopper Stabilized amplifiers are superlative in both offset voltage and current drift with time and temperature. Precision integration is one application which requires both very low voltage and current offsets. Signals in the low microvolt region can be successfully amplified with chopper stabilized amplifiers. Unlike differential type amplifiers, chopper stabilized amplifiers are relatively immune to offsets due to thermal gradients. Most of these devices have single - ended inputs which limits their application to the inverting connection.

Varactor Bridge (or Parametric) - The varactor bridge amplifier achieves offset current and drift of one to two orders of magnitude lower than FET's. As for FETs, offset voltage drift performance is only moderate. This amplifier is useful in electrometer applications where voltages and currents must be measured from source impedances in the range from 10^8 to 10^{12} ohms. Integrators with time constants of several hours can be designed. Low frequency noise is exceptionally good since 1/f noise is virtually eliminated.

	$\frac{\Delta e_{os}}{\Delta T}$ uV/°C	$\frac{\Delta e_{os}}{\Delta t}$ uV/day	$\frac{\Delta i_{os}}{\Delta T}$ pa/°C	$\frac{\Delta i_{os}}{\Delta t}$ pa/day	I_{os} pa
Differential Transistor	3 to 30	5 to 100	200 to 2000	50 to 5000	1000 to 200,000
Differential F.E.T.	15 to 50	25 to 100	*	.1 to 1	50 to 150
Chopper Stabilized	0.2 to 5	0.5 to 10	0.5 to 10	0.5 to 10	10 to 100
Varactor Bridge	30 to 100	50 to 100	*	.01 to .1	1 to 10

*I_{os} doubles every 10°C, 1pa=10^{-12}amps

Fig. 14 — Typical Drift Performance

ANALOG DEVICES

OPERATIONAL AMPLIFIERS

221 FIFTH STREET, CAMBRIDGE, MASS., 02142

	HIGH PERFORMANCE DIFFERENTIAL			*LOW COST DIFFERENTIAL*		
	Excellent time drift, low initial voltage offset, high input impedance, low input current, high gain and selection of voltage drifts to 5uV/°C			For greatest economy without the usual sacrifice in gain, drift and output current. AC gain of 94db to 1KC on 106/107.		
SPECIFICATIONS (typical @ 25°C unless otherwise noted.)	**101 A/B/C** Wideband Inverting ±8 to 16V Power Supply 5ma Output Current	**102 A/B/C** Wideband Noninverting Very High Gain—20ma Fast Slewing Rate	**103 A/B/C** Low Frequency 20ma Output Current ±8 to 16V Power Supply	**106/L106** 5ma Output Current High Gain Excellent AC ampl.	**107/L107** 5ma Output Current High Gain Reduced Input Current	**108/L108** Low Frequency Lowest Input Current High Input Impedance
OPEN LOOP GAIN @ DC, rated load, min.	10^5	2×10^6	10^5	1.5×10^5	1.5×10^5	5×10^4
RATED OUTPUT Voltage, min.	±11V	±11V	±11V	±10V	±10V	±10V
Current, min.	5ma.	20ma.	20ma.	5ma.	5ma.	2.5ma
FREQUENCY RESPONSE Unity gain, small signal	10mc	10mc	500KC	1.5mc	1.5mc	500KC
Full Output Voltage	30KC	300KC	2KC	20KC	20KC	2KC
Slewing Rate	2V/μsec	30V/μsec	0.13V/μsec	1.2V/μsec	1.2V/μsec	0.12V/μsec.
Overload Recovery	200μsec	—	5msec.	1msec	1msec	5msec
INPUT VOLTAGE OFFSET Initial Offset, @ 25°C, max.[1]	±1mV	±1mV	±1mV	—	—	—
Avg. vs. temp., max.[5]	Models A — 20μV/°C, B — 10μV/°C, C — 5μV/°C			20μV/°C	20μV/°C	20μV/°C
vs. supply voltage, max.	15μV/%	10μV/%	15μV/%	20μV/%	20μV/%	20μV/%
vs. time	10μV/day	10μV/day	10μV/day	50μV/day	50μV/day	50μV/day
INPUT CURRENT OFFSET Initial Offset, @ 25°C, max.	±2na	±2na	±2na	±150na	±20na.	±2na
Avg. vs. temp., max.[5]	0.2na/°C	0.4na/°C	0.2na/°C	1.5na/°C	1.5na/°C	0.3na/°C
vs. supply voltage.	0.15na/%	0.15na/%	0.15na/%	2na/%	2na/%	0.3na/%
INPUT IMPEDANCE Between Inputs	4MΩ	6MΩ	4MΩ	100KΩ	100KΩ	4MΩ
Common Mode	500MΩ	500MΩ	500MΩ	50MΩ	50MΩ	500MΩ
INPUT VOLTAGE Max. Between Inputs	±15V	±15V	±15V	±15V	±15V	±15V
Max. Common Mode	±10V	±10V	±10V	±10V	±10V	±10V
Common Mode Rejection	20,000	20,000	20,000	20,000	20,000	20,000
INPUT NOISE Voltage, DC to 1CPS, P to P	—	—	—	—	—	—
5 to 50KC, RMS	4μV	8μV	4μV	4μV	4μV	4μV
Current, DC to 1CPS, P to P	—	—	—	—	—	—
POWER SUPPLY Voltage	±(8 to 16) VDC[2]	±(15 to 16) VDC	±(8 to 16) VDC[2]	±(15 to 16) VDC	±(15 to 16) VDC	±(15 to 16) VDC
Current, rated load	20ma.	35ma.	30ma.	15ma.	15ma.	5ma.
CASE SIZE	Fig. 1	Fig. 1	Fig. 1	Fig. 2/Fig. 1	Fig. 2/Fig. 1	Fig. 2/Fig. 1
PRICE	A B C	A B C	A B C	106 L106	107 L107	108 L108
1-9	$68 78 98	95 105 120	74 84 104	26 30	31 35	35 40
10-24	$66 75 95	92 102 116	71 81 101	25 29	30 34	33 37

NOTES

Note 1 — Adjustable to zero with external pot

Note 2 — Specifications given for ±15VDC

Note 3 — Maximum operating and storage temperature is 75°C

Note 4 — 0.06pa/°C from 0 to 50°C

Note 5 — Averaged over —25 to +85°C

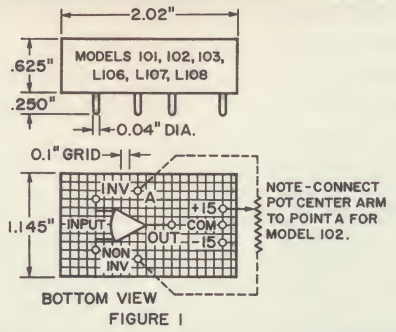

FIGURE 1

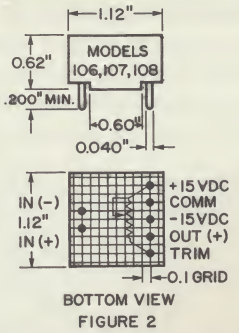

FIGURE 2

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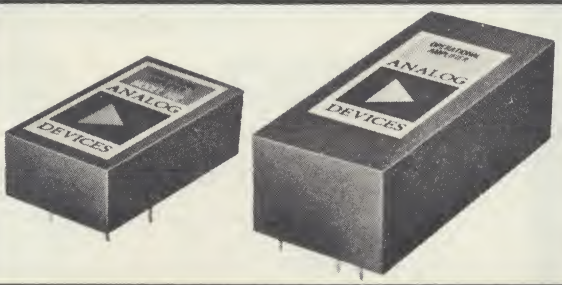

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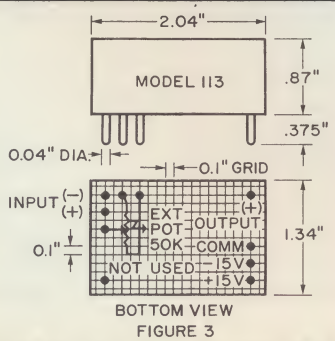
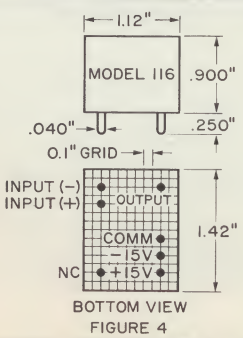
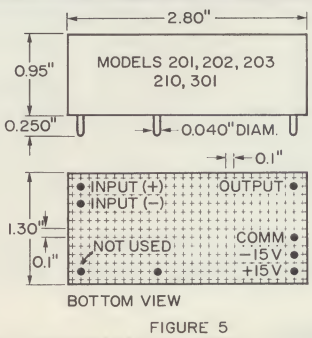
113 **High Gain** **Low Drift** **High Input Impedance**	**116** **Low Noise** **Excellent AC ampl.** **Fast Recovery**	**201** **100ma Output Current** **Wideband** **Ultra Low Drift**	**202** **Wideband — 20ma** **Fast Slew Rate** **Ultra Low Drift**	**203** **Low Noise — 20ma** **Low Frequency** **Ultra Low Drift**	**210** **Low Cost — 20ma** **Very Fast Slew Rate** **Low Noise**	**301** **High CM Voltage** **Very High Zin** **Very Low Noise**
2×10^6	10^5	10^9	10^9	10^8	10^8	10^6
±11V 100ma	±11V 100ma.	±11V 100ma.	±11V 20ma.	±11V 20ma.	±10V 20ma.	±10V 20ma.
10mc 300KC 30V/μsec —	10mc 500KC 30V/μsec 0.2μsec	10mc 500KC 30V/μsec 0.5μsec.	10mc 500KC 30V/μsec 0.5μsec.	2mc 20KC 1.2V/μsec 5μsec.	20mc 500KC 100V/μsec 0.2μsec.	500KC 5KC 0.3V/μsec 200μsec
±1mV 20μV/°C 2μV/% 10μV/day	±10mV 100μV/°C — —	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±20μV 0.2μV/°C[3] 0.4μV/% 1μV/day	±100μV 1μV/°C 10μV/% 1μV/day	— 30μV/°C 30μV/% —
±1na 0.2na/°C —	±300na. 40na/°C —	50pa 0.5pa/°C[3] 1pa/%	50pa 0.5pa/°C[3] 1pa/%	50pa 0.5 pa/°C[3] 1pa/%	100pa. 2pa/°C 10pa/%	±1pa 0.3pa/°C[4] .001pa/%
7 MΩ 500MΩ	20KΩ 2.5MΩ	220KΩ N.A.	220KΩ N.A.	220KΩ N.A.	500KΩ N.A.	10^{10}Ω, 500pf 10^{12}Ω, 10pf
±15V ±10V 20,000	±15V ±10V —	±15V single ended	±15V single ended	±15V single ended	±15V single ended	±20V ±300V 10^8
— 8μV —	— 3μV —	25μV 10μV 20pa	25μV 10μV 20pa	10μV 10μV 10pa	5μV 10μV 10pa	1μV — .01pa
±(15 to 16) VDC 150ma.	±(15 to 16) VDC 150ma.	±(15 to 16) VDC 150ma.	±(15 to 16) VDC 50ma.	±(15 to 16) VDC 50ma.	±(15 to 16) VDC 60ma.	±(15 to 16) VDC 35ma.
Fig. 3	Fig. 4	Fig. 5	Fig. 5	Fig. 5	Fig. 5	Fig. 5
$195 $185	98 95	270 256	235 224	215 205	157 148	198 193



BOTTOM VIEW
FIGURE 3

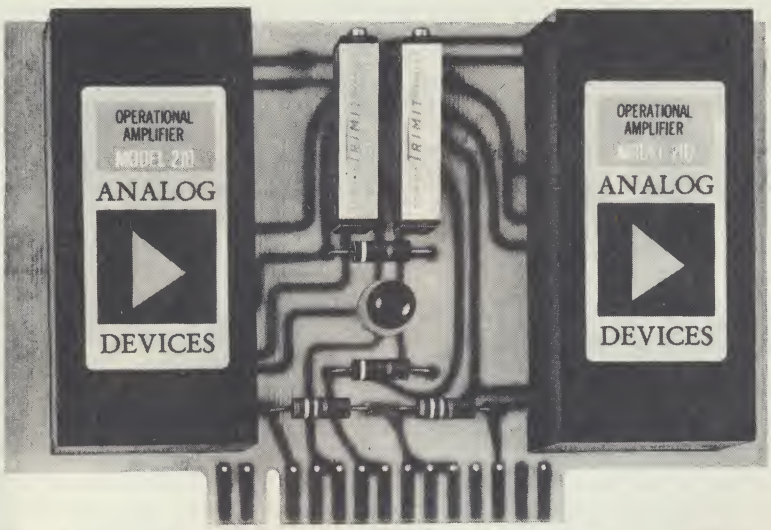


BOTTOM VIEW
FIGURE 4



BOTTOM VIEW
FIGURE 5

WRITE FOR ANALOG DEVICES' COMPLETE DATA ON ALL OF AMPLIFIERS ILLUSTRATED



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AN OPERATIONAL AMPLIFIER APPLICATION MANUAL

OPERATIONAL AMPLIFIERS

PART I — Principles of operation and analysis of errors.

PART II — Inverting, non-inverting and differential configurations.

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OPERATIONAL AMPLIFIERS, PART I

Principles of operation and analysis of errors

Ray Stata, Vice President
Analog Devices, Inc., Cambridge, Mass.

The term "operational amplifier" was orginally coined by those in the analog computer field to denote an amplifier circuit which performed various mathematical operations such as integration, differentiation, summation and subtraction. Although operational amplifiers are still widely used for analog computation, the application of these devices has been so vastly extended that the terminology is now archaic. Today, the widest use of operational amplifiers is in such applications as signal conditioning, servo and process controls, analog instrumentation and system design, impedance transformation, voltage and current regulators and a host of other routine functions.

Non-linear applications of operational amplifiers have also been added to the growing frontier of analog amplifier technology. In this category, operational amplifiers are used for voltage comparators, A to D and D to A converters, logarithmic amplifiers, non-linear function generators and ultra-linear rectifiers, to name only a few applications.

An operational amplifier is generally characterized by the following properties:

- Extremely high dc voltage gain, generally in the range from 10^4 to 10^9.
- Wide bandwidth starting at dc and rolling off to unity gain at from 1 to 100 Mc/s with a slope of 6 db/octave or at most 12 db/octave.
- Plus and minus output voltage over a large dynamic range, generally from ± 10 to ± 100 v.
- Very low input dc offset and drift with time and temperature.
- High input impedance so that amplifier input current can be largely neglected.

The great versatility and many advantages of operational amplifiers stems from the use of negative feedback. You recall from circuit theory that negative feedback tends to improve gain stability, to reduce output impedance, to improve linearity and in some configurations, to increase input impedance. As shall be pointed out later, the extent to which closed loop performance is improved by negative feedback, depends on the magnitude of loop again ($A\beta$).

Another useful property of negative feedback, which is the basis for all operational amplifier technology, is that with enough gain, the closed loop amplifier characteristics become a function of only the feedback components. For example, the gain of the closed loop circuit in Fig 1 is determined almost entirely by the ratio of the two resistors, Z_f/Z_i and is largely independent of the open loop characteristics of the operational amplifier. Since the selection and configuration of the feedback components determine the operation of the circuit, the versatility in applying operational amplifiers is limited primarily by your ingenuity in selecting and configuring the feedback components.

OPERATIONAL AMPLIFIER CHARACTERISTICS

An ideal operational amplifier would have infinite open loop gain and bandwidth and zero input noise, offset and drift. In this case the feedback components determine entirely the closed loop performance and the operational amplifier has absolutely no effect on the circuit performance. Although, of course, no amplifier has these ideal qualities, the performance of modern solid state amplifiers closely approaches these limits. To discuss the limitations of practical amplifiers and how these limitations effect closed loop performance, the errors due to the non-ideal characteristics of operational amplifiers are classified into four basic categories:

- Static errors due to finite amplifier gain.
- Dynamic errors due to bandwidth limitations.
- Errors due to initial voltage and current offsets and drift caused by temperature change, time stability and supply voltage change.
- Errors due to noise.

There are also more refined considerations such as common mode voltage characteristics and finite input and output impedances which effect the performance of operational amplifier circuits.

Static Errors Due to Finite Amplifier Gain

The most distinguishing feature of operational amplifiers is the staggering magnitude of dc voltage gain which they boast. Even the least expensive differential amplifiers have voltage gains of 10^4 while high performance chopper stabilized units have gains as high as 10^9. Negative feedback around this high voltage gain, accomplishes the virtues of closed loop performance and

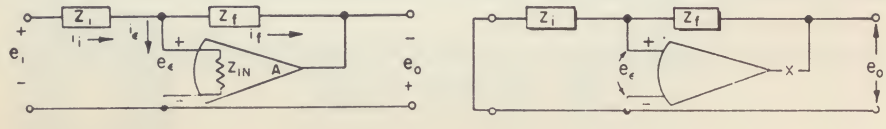


Fig 1 (Left) — Operational amplifier circuit. Fig 2 (Right) — Circuit to determine the feedback attenuation β.

makes the circuit dependent only on the feedback components.

Before proceeding to a mathematical analysis of operational circuit performance, it is interesting to intuitively examine the significance of voltage gain. Suppose, as an extreme case, you assume that the amplifier in Fig 1 has a dc voltage gain of 10^8 and a maximum output voltage ± 10 v dc. In all other regards, suppose that the amplifier is ideal which among other things implies that $e_o = o$ when $e_i = o$. You can then state that when the output voltage swings through its extremes of $+10$ to -10 v dc, the error voltage, e_ϵ, will not vary by more than ± 0.1 μv from ground. The currents through Z_i and Z_f are then:

$$i_i = (e_i - e_\epsilon)/Z_i \approx e_i/Z_i \qquad (1)$$

$$i_f = (e_\epsilon - e_o)/Z_f \approx -e_o/Z_f \qquad (2)$$

To go further, let us say that in this circuit the ratio of Z_f/Z_i is selected so that the output voltage will be $+10$ v dc when the input is -10 mv which states that the closed loop gain, e_o/e_i, is 1000. Since the error voltage will not exceed 0.1 μv, e_ϵ is completely negligible compared to e_o and an error of less than 0.001% (0.1 μv/10 mv), is committed by neglecting e_ϵ as compared to e_i. Assuming that $e_\epsilon = o$, implies that $i_\epsilon = 0$, which, for any practical value of Z_{IN}, is an excellent assumption. If $i_\epsilon = o$, then,

$$i_i = i_f \qquad (3)$$

From Eqs (1) and (2), the closed loop gain, determined entirely by the ratio of Z_f and Z_i, is:

$$e_o/e_i = -Z_f/Z_i \qquad (4)$$

This simple example shows the validity of two basic assumptions which underlie the analysis of all operational amplifier circuits, namely:

- Feedback current, i_f, is equal to the input current, i_i, since error current, i_ϵ, is negligible.
- The error voltage, e_ϵ, across the operational amplifier input terminals is assumed to be zero volts.

To repeat, these assumptions follow from the fact that negative feedback, coupled with high open loop gain, constrains the error voltage and consequently the error current to infinitesimal values. The higher the gain, the more valid these assumptions become.

Quantitative Gain Error Analysis: To develop quantitative expressions for the errors caused by finite amplifier gain, assume that the amplifier in Fig 1 is ideal except for finite gain. These assumptions can be stated quantitatively as:

$$Z_{IN} = \infty,\ e_o = o \text{ when } e_i = o$$

$$Z_{out} = o,\ \omega_o = \infty \ (\textit{infinite bandwidth})$$

For an amplifier with open loop voltage, A, the exact closed loop gain is,

$$\frac{e_o}{e_i} = -\underbrace{\left[\frac{Z_f}{Z_i}\right]}_{\substack{\textit{ideal}\\ \textit{amplifier}}} \underbrace{\left[\frac{1}{1+(1/A)(1+Z_f/Z_i)}\right]}_{\substack{\textit{error factor due}\\ \textit{to finite voltage gain}}} \qquad (5)$$

As the gain, A, approaches infinity, eq (5) reduces to the form of an ideal operational circuit:

$$e_o/e_i = -Z_f/Z_i \qquad (6)$$

Consequently, the error in closed loop gain, e_o/e_i, due to finite open loop gain, A, is:

$$\textit{error factor} = \frac{1}{1+(1/A)(1+Z_f/Z_i)} \qquad (7)$$

If we let $1/\beta = 1 + Z_f/Z_i$ eq (7) can be rewritten

$$\textit{error factor} = \frac{1}{1+1/A\beta} \approx 1 - 1/A\beta, \textit{ for } A\beta >> 1$$

The error factor is in a form which, when multiplied by the ideal closed gain, gives the actual closed loop gain. The percentage error due to finite gain A is:

$$\varepsilon(\%) = 100/A\beta \qquad (8)$$

Gain Stability: Closed loop gain error, eq (8), is not in itself tremendously important since the ratio Z_f/Z_i can always be adjusted to compensate for this error. However, closed loop gain stability is an important consideration in most applications. Closed loop gain stability is effected primarily by variations in open loop gain due to changes in temperature and load or due to aging of amplifier components. Redefining closed loop gain by $G_{cl} = e_o/e_i$, then

$$\frac{\Delta G_{cl}}{G_{cl}} \approx \frac{\Delta A}{A} \quad \frac{1}{A\beta} \qquad (9)$$

From eq (9) any variation in open loop gain, A, is reduced by the factor Aβ in its effect on closed loop gain, G_{cl}. Improvement in gain stability is one of the important benefits of negative feedback.

Loop Gain

The product Aβ which occurs in eqs (8) and (9), is called loop gain, a well known term in feedback theory. The improvement in closed loop performance due to negative feedback is, in nearly every case, proportional to loop gain.

To a first approximation, closed loop output impedance, linearity and gain stability, are all reduced by Aβ with negative feedback. Term β, generally called feedback attenuation, is defined as the factor by which the output voltage, e_o, is attenuated to produce the error voltage, e_ϵ, with the forward gain open and with the input source replaced by its Thevin equivalent resistance. Assuming zero source resistance, by definition $1/\beta$ from the circuit in Fig 2 is:

$$\frac{\Delta e_o}{\Delta e_\epsilon} = \frac{Z_i + Z_f}{Z_i} = 1 + \frac{Z_f}{Z_i} = \frac{1}{\beta} \qquad (10)$$

For $Z_f > Z_i$, which is generally the case for closed loop gain greater than one:

$$1/\beta \approx Z_f/Z_i = e_o/e_i = G_{cl} \qquad (11)$$

Consequently, loop gain, Aβ, is approximately the ratio of open loop gain to closed loop gain,

$$A\beta \approx A/G_{cl}$$

This discussion emphasizes that the loop gain is the significant factor in predicting the performance of closed loop operational amplifier circuits. The open loop gain required to obtain an adequate amount of loop gain will, of course, depend on the desired closed loop gain. For example, an amplifier with an open loop gain of 20,000 will have a loop gain of 2000 for a closed loop gain of 10, but only a loop gain of 20 for a closed loop gain of 1000.

Frequency Dependence of Loop Gain: Thus far, it was assumed that the open loop gain is independent of fre-

quency. Unfortunately, this is not the case. Leaving the discussion of the effect of open loop response on bandwidth and dynamic errors until later, let us now investigate the effect of frequency response on loop gain and static errors.

The open loop frequency response for a typical operational amplifier with superimposed closed loop amplifier response for a gain of 100 or 40 db, illustrates graphically (Fig 3) these results:

- Loop gain in db is the difference between open loop gain and closed loop gain. Actually loop gain is the ratio between open and closed loop gain, but subtracting on a logarithmic scale is equivalent to normal division.
- Loop gain decreases with increasing frequency due to the attenuation of open loop gain.
- Loop gain decreases for higher values of closed loop gain.
- Closed loop gain depends entirely on the ratio of the feedback components, Z_f and Z_i, and is independent of open loop gain (apart from errors which are inversely proportional to loop gain).
- Where the closed loop and open loop curves intersect, loop gain is zero which implies that beyond this point, there is no negative feedback. Consequently, closed loop gain will be equal to open loop gain.

Fig 3 points out that the high open loop gain quoted for operational amplifiers is somewhat misleading. Beyond a few c/s, open loop gain is attenuated rapidly. Consequently, closed loop gain stability, output impedance, linearity and other parameters which depend on loop gain, are degraded at higher frequencies. One of the reasons for having dc gain as high as 10^5 and bandwidth as wide as several Mc/s, is to obtain adequate loop gain at frequencies even as low as 100 c/s.

One approach to improving loop gain at high frequencies other than by increasing open loop gain is to increase open loop bandwidth. Fig 4 illustrates the improvement in loop gain obtained by increased bandwidth. Another approach to improving loop gain at higher frequencies, is to have faster attenuation of the open loop response. Normally, operational amplifiers have 6 db/octave attenuation to provide stable operation for all values of resistive feedback. While it is true that fast roll-off amplifiers are more difficult to stabilize, once the techniques for applying amplifiers with these characteristics are understood, it is just as easy to use them and the high frequency performance is considerably improved over conventional 6 db/octave amplifiers. Fig 5 illustrates the improvement obtained in loop gain at high frequencies by using a fast roll-off amplifier.

Generalized Operational Circuit With Multiple Inputs

In the foregoing analysis the impedances Z_i and Z_f have been used to denote that the feedback elements may be any linear, passive, bilateral networks. These impedances may be complex. For purposes of amplification or isolation, the feedback elements would be resistors, but in other applications such as servo controls, the feedback elements may be rather complicated networks. The same analyses are applicable to non-linear feedback elements such as diodes or transistors.

In the most general cases, it is possible to sum or otherwise manipulate a number of input voltages as shown in Fig 6. In this configuration, the inputs are almost completely isolated from each other due to the very low error voltage at the summing junction.

The generalized closed loop gain equation for this circuit is:

$$e_o = (\textit{ideal amplifier})\ (\textit{error factor due to finite gain}) \tag{12}$$

where:

$$(\textit{ideal amplifier}) = e_1 \frac{Z_f}{Z_1} + e_2 \frac{Z_f}{Z_2} + \ldots + e_N \frac{Z_f}{Z_N}$$

$$\textit{and } (\textit{error factor}) = \frac{1}{1 + (1/A)\left(1 + \frac{Z_f}{Z_1} + \frac{Z_f}{Z_2} + \ldots + \frac{Z_f}{Z_N}\right)}$$

$$\textit{or } e_o = -\left[\sum e_i \frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + (1/A)(1 + Z_f/Z_p)}\right]$$

where Z_p is the parallel sum of $Z_1, Z_2 \ldots . Z_N$.
For any one input voltage eq (12) reduces to the form of eq (6),

$$\frac{e_o}{e_i} = -\left[\frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + \frac{1}{A\beta_p}}\right]$$

Except now,

$$1/\beta_p = 1 + \frac{Z_f}{Z_p}$$

All of the preceding discussions and results are equally applicable to the circuit in Fig 6, except that loop gain, $A\beta_p$, for this case may be considerably reduced due to the parallel sum of the input impedances. The errors due to finite loop gain will be increased by the ratio β/β_p. Since the loop gain for all inputs is the same, if any one input impedance is low, the ensuing errors for all other inputs are also increased.

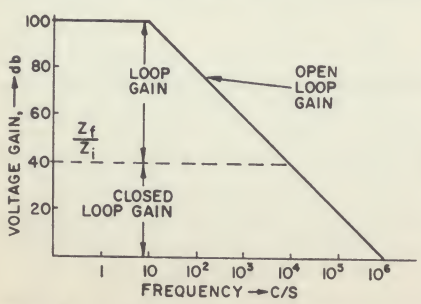


Fig 3 — Open loop frequency response.

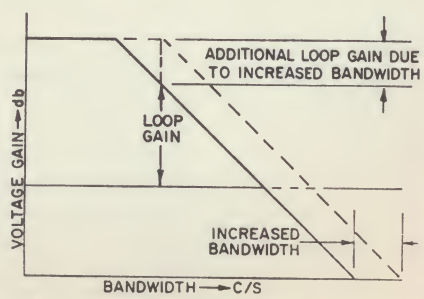


Fig 4 — Effect of increased bandwidth on loop gain.

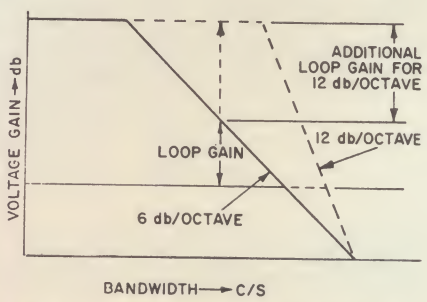


Fig 5 — Comparison of loop gain for 6 db/ and 12 db/ octave amplifiers.

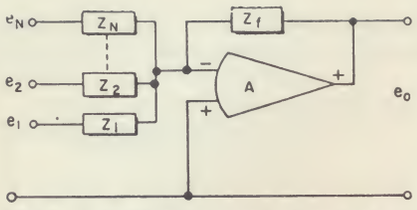
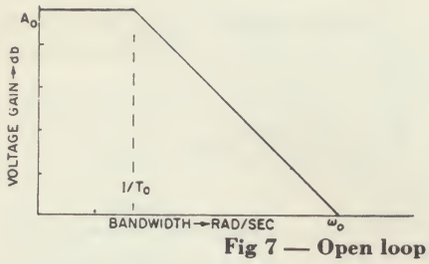


Fig 6 — Multiple input summing amplifier.



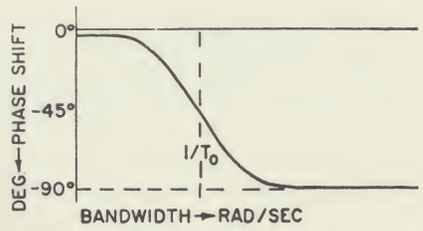


Fig 7 — Open loop gain phase response.

Frequency Response and Dynamic Errors

We have already mentioned that nature imposes some restrictions on the maximum achievable bandwidth for operational amplifiers. Typical amplifiers have unity gain bandwidth of 1 Mc/s with some special amplifiers having bandwidths as high as 100 Mc/s. Since operational amplifiers almost invariably employ large amounts of negative feedback, the attenuation of open loop response must satisfy certain requirements to insure stable closed loop operation. H. N. Bode in his "Network Analysis and Feedback Amplifier Design", D. Van Nostrand, Princeton, New Jersey 1951 showed that closed loop operation will be stable if the log plot of open loop gain exhibits a slope of less than—12 db/octave in the region of crossover.

Operational amplifiers are usually designed to have attenuation of 6 db/octave to assure that closed loop operation will be stable for all possible values of resistor feedback with the usual stray capacitance, load capacitance and input capacitance which are present in a circuit. However, there are advantages to be gained from amplifiers designed for 12 db/octave attenuation. The stability problem for these amplifiers can be solved, once a few basic application techniques are understood.

Fig 7 gives a very close approximation to the open loop gain-phase characteristics of a 6 db/octave amplifier. Mathematically, the amplifier behaves like a simple linear first order lag.

$$A(S) = A_o/(1 + T_oS), \text{ where } S = j\omega$$

For frequencies greater than $s = 1/T_o$, gain becomes,

$$A(S) = A_o/T_oS = \omega_o/S \qquad (14)$$

Substituting eq (14) for A in eq (5) the dynamic closed loop gain response for the circuit in Fig 1 becomes:

$$e_o/e_i = -\left[\frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + \frac{S}{\omega_o}\left(1 + \frac{Z_f}{Z_i}\right)}\right] \qquad (15)$$

$$= -\left[\frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + T_cS}\right]$$

$$\text{where } T_c = [1 + Z_f/Z_i]/\omega_o = 1/\beta\omega_o \qquad (16)$$

Fig 8 illustrates the dynamic closed loop gain response given by eq (15). The closed loop bandwidth is directly proportional to open loop bandwidth ω_o and is inversely proportional to closed loop gain. This is another way of stating that the gain-bandwidth product for a feedback amplifier is constant. As closed loop gain is increased, bandwidth is decreased.

Transient Response: The closed loop step response for eq (15) is a simple exponential with time constant T_c:

$$e_o(t) = (-Z_f/Z_i)(1 - e^{-t/T_c})$$
$$\text{for } e_i = \mu_{-1}(t)$$

The time constant, T_c, eq (16), increases for increasing values of closed loop gain and decreases for increasing values of open loop bandwidth, ω_o. Fig 9 shows the step function response together with the time required to reach various percentages of the final values.

As an example, the time required for a one Mc/s unity gain (ω_o) amplifier connected for a closed loop gain of 100 to reach 0.1% of its final value after a step input,

$$T = 6.9T_c = 6.9(100/6.28 \times 10^6) = 110\ \mu\text{sec}$$

Rate Limiting, Slewing Rate and Full Output Frequency Response: Another limitation to transient response is rate limiting. Apart from bandwidth, operational amplifiers have limitations on the maximum rate of change of output voltage which will not permit the amplifier to respond as fast as the amplifier time constant might indicate. This tends to be a problem for large input voltage steps.

The maximum full output frequency is usually given by the manufacturers to define this limitation. Alternatively, a specification for maximum slewing rate is sometimes given, generally in volts/μsec. Slewing rate and full output frequency are related as follows: for a sine wave, the maximum output voltage for full output frequency, ω_{fo}.

$e_o(t) = A_p \sin \omega_{fo} t$, *where* A_p *is the peak output voltage*

The maximum rate of change of this voltage or slewing rate is,

$$(de_o/dt)_{max} = A_p\omega_{fo}/10^6 \text{ volts}/\mu\text{sec}$$

Fast Roll-Off Amplifier: Not only do fast roll-off amplifiers provide more loop gain at high frequencies as previously discussed, but they also offer wider closed loop bandwidth for a given unity gain crossover frequency. Fig 10 shows a comparison of the closed loop bandwidths obtainable for a 6 db/octave and a 12 db/octave amplifier. Stable closed loop performance can be obtained for a 12 db/octave amplifier by the addition of a lead capacitor in the feedback network as shown in Fig 11. The effect of the lead capacitor on closed loop response is illustrated in Fig 12. So long as the rate of

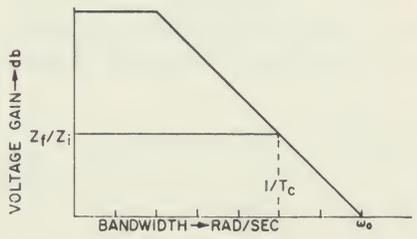


Fig 8 — Closed loop frequency response.

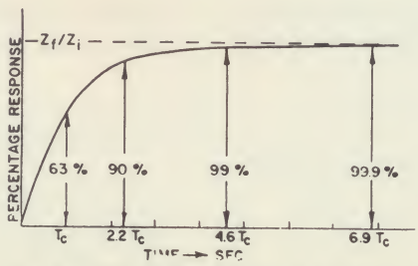


Fig 9 — Closed loop step response.

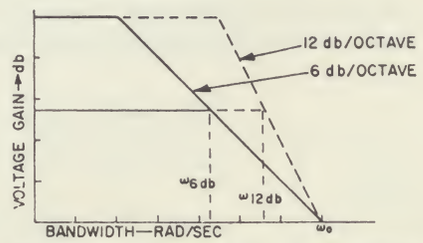


Fig 10 — Comparison of bandwidth for 6 and 12 db/ octave amplifiers.

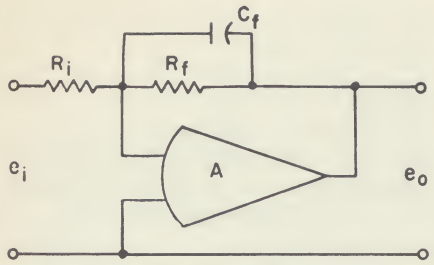


Fig 11 — Stabilization with feedback capacitor.

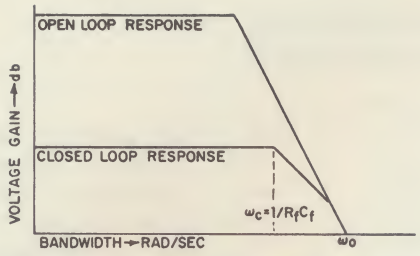


Fig 12 — Frequency response with feedback capacitor.

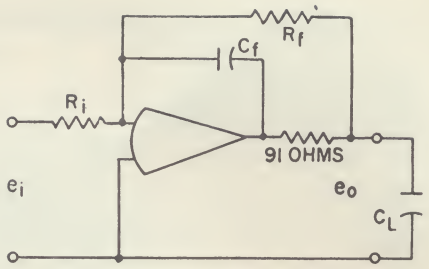


Fig 13 — Isolation of load capacitance.

closure between the open loop and closed loop response curves is less than 12 db/octave, the closed loop response will be stable. The location of the compensating break frequency, ω_c, establishes the closed loop phase margin.

Fig 13 illustrates a technique for isolating load capacitance which may cause oscillations for a 12 db/octave amplifier. Since the load isolation resistor is inside the feedback loop, low output impedance is maintained. These illustrations are intended to indicate that in most applications, a 12 db/octave amplifier can be stabilized as well as a 6 db/octave amplifier and at the same time, the benefits of increased loop gain at high frequencies and wider closed loop frequency response are obtained.

Overload Recovery: Another source of dynamic error is the overload recovery time after the amplifier has been saturated. Chopper stabilized amplifiers, by their very design, have notoriously long overload recovery times: up to 3 minutes. Differential amplifiers are in general much better in this respect with recovery times in the range from 5 to 50 msecs. Moreover, 12 db/octave amplifiers tend to recover faster than 6 db/octave amplifiers and may have recovery times as short as 200 μsec.

A remedy for the overload recovery problem is to include a circuit in the feedback loop which prevents the output from reaching the saturation voltage. One such clamping circuit is shown in Fig 14. This circuit has a response of a few μsec so that recovery time is generally limited only by the closed loop bandwidth of the amplifier. In addition, this configuration limits the leakage current through the feedback network to something less than 10 pa, depending on the quality of the diodes.

Input Offset and Drift Errors

Although an ideal amplifier has exactly zero output voltage for zero input voltage, any practical dc amplifier invariably exhibits an input offset. Offset in itself is generally not a serious problem since you may compensate for it with various techniques by artificially injecting an equal and opposite signal at the summing junction. However, any tendency for the offset to drift either due to temperature change, time or supply voltage variations, presents a basic limitation since this drift would necessitate the compensating signals to be constantly readjusted. One important figure of merit for an operational amplifier is the magnitude of offset drift.

Offset drift falls into two separate and distinct categories. One cause of drift can be characterized by a voltage source connected in series with the summing junction, Fig 15, while another source of drift can only be characterized by a current source in parallel with the summing junction. To successfully apply operational amplifiers the distinction between these two sources of drift must be understood in order to predict their effect on circuit performance.

Voltage Offset and Drift: The principal causes for voltage drift are changes in ambient temperature and supply voltage or long term stability due to component aging. Less obvious and more uncommon sources of voltage offset are self heating due to load variations and rectification of high frequency overdrive signals. Encapsulated amplifiers offering higher output voltage or current ratings are subject to considerable internal dissipation which may generate enough heat to cause the input to drift as the load is changed. Input signals which contain frequency components that exceed the amplifier bandwidth or rate limiting capabilities may be rectified and cause an offset referred to the input.

Voltage drift due to ambient temperature change is generally specified as the average drift over a given temperature range. This can be somewhat misleading. For example, Fig 16 shows a voltage offset vs temperature for a particular amplifier. Although the curve falls within the specification limits, the slope of the curve at any one temperature may exceed the average drift rate. A more precise way of specifying drift is to give the maximum total voltage change over the temperature range of interest.

Another anomaly in specifying temperature drift is that the ratings given are for steady state temperature conditions. The drift performance, particularly for differential type amplifiers, depends on precisely matching the temperature effects of the input transistors. Successful operation then depends on the components within the circuit being maintained at exactly the same temperature. Encapsulated amplifiers use potting compounds with low thermal resistance which tends to minimize thermal unbalance. However, in applications where thermal gradients are prevalent in the vicinity of the amplifier, it is possible to obtain voltage offset transients which exceed the steady state drift specifications by an order of magnitude. Chopper

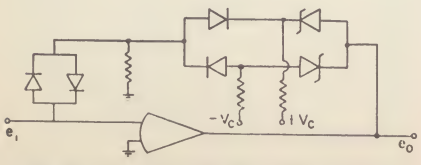


Fig 14 — Overload recovery circuit.

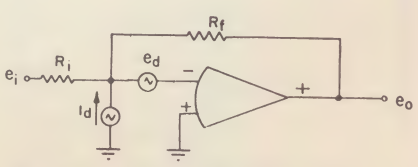


Fig 15 — Sources of offset drift.

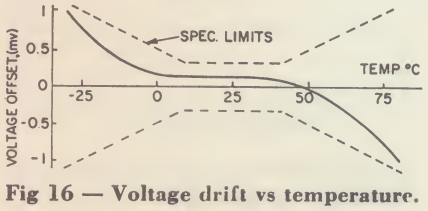


Fig 16 — Voltage drift vs temperature.

type amplifiers are relatively insensitive to thermal gradients and they should be considered in environments which present this problem.

Voltage source drift referred to the output for the circuit in Fig 15 is given by,

$$\Delta e_o = e_d/\beta = e_d(1 + R_f/R_i)$$

$$\Delta e_o \approx e_d R_f/R_i, \text{ for } R_f >> R_i \qquad (17)$$

where e_d is the total offset voltage change over the time, temperature and supply voltage range of interest. Eq (17) follows directly from eq (11) where it was indicated that the output is always $1/\beta$ times the error voltage at the summing junction. Since e_d can be considered another form of error voltage the same eq (11) is applicable.

Offset drift is defined in terms of the voltage required at the input to rezero the output. Thus drift referred to the input is obtained by dividing the output drift eq (17) by the closed loop gain, R_f/R_i,

$$\Delta e_i = (e_d/\beta)(R_i/R_f) = e_d(1 + R_f/R_i)(R_i/R_f)$$

$$\Delta e_i \approx e_d, \text{ for } R_f >> R_i \qquad (18)$$

It is important to note that the usual approximations for voltage source drift referred to the input and output as given by eq (17) and eq (18) can lead to substantial errors for low values of closed loop gains. To illustrate this point, the table, Fig 17 gives the exact values for input and output drift for various values of closed loop gain, R_f/R_i, for an amplifier with $e_d = 20$ μv/°C.

Closed Loop Gain R_f/R_i	Input Drift, μv/°C $e_i = e_d(1 + R_f/R_i)(R_i/R_f)$	Output Drift, μv/°C $e_o = e_d(1 + R_f/R_i)$
1	40	40
2	30	60
3	26	80
4	25	100
5	24	120
10	22	220
100	20.2	2020

Fig 17 — Voltage drift vs closed loop gain.

Current Offset and Drift: The discussion of voltage offset and drift in the previous section is applicable to current offset and drift as well, except for one important difference. Unlike voltage source drift, the effect of current drift depends on the magnitude of the feedback components since any current which is pumped into the summing junction is inherently balanced out by an equal and opposite current which forced through the feedback impedance, Z_f. Consequently, the uncertainty in output voltage due to a change in offset current i_d, is:

$$\Delta e_o = i_d R_f$$

By dividing the output voltage by closed loop gain, the uncertainty referred to the input is:

$$\Delta e_i = e_o/(R_f/R_i) = i_d R_i$$

Thus, to obtain the effect of current drift referred to the input, multiply the current drift by the summing impedance, R_i.

Current Drift Compensation: For differential type amplifiers it is possible in some applications to partially compensate for current drift. This follows as actually, each input of the amplifier has an effective parallel current drift source as shown in Fig 18. The current drift and offset at each input tend to track with changes in temperature, time and supply voltage. Therefore, if the impedance in each leg is balanced, the effect of current drift and offset tend to be cancelled.

The circuit in Fig 18, illustrates the connections for current drift compensation. For this circuit the current drift at the output is:

$$\Delta e_o = -i_{d2}(R_c)(R_i + R_f)/R_i + i_{d1}(R_f)$$

For the case where $R_c = R_f R_i/(R_i + R_f)$ this becomes:

$$\Delta e_o = R_f(i_{d1} - i_{d2})$$

Dividing the output drift by the closed loop gain $(-R_f/R_i)$, gives the drift referred to the inputs as:

$$\Delta e_i = R_i(i_{d2} - i_{d1})$$

Consequently, if the two current sources are exactly equal in magnitude and R_c is chosen correctly, current drift is entirely cancelled. Although this is never quite the case, at the extreme of operating temperatures where current drift is worst, you can obtain by this technique an improvement in current drift approaching a factor of ten.

Combined Voltage and Current Drift: Total drift, which is obtained by combining voltage and current drift, referred to input and output is:

$$\Delta e_i = e_d + i_d R_i \text{ and}$$

$$\Delta e_o = e_d \frac{R_f}{R_i} + i_d R_f, \text{ for } R_f >> R_i$$

It is informative to illustrate by an example, the relative importance of voltage and current drift. The chart, Fig 19 gives the total drift referred to the input of a typical differential amplifier with average voltage and current drift of 25 μv/°C and 0.5 na/°C respectively. Total drift is given for various values of summing resistor R_i.

Input drift for low impedance circuits is thus primarily due to voltage source drift, while for high impedance circuits, input drift is primarily due to current source drift. In conclusion, you must consider both the voltage and current source drift, together with impedance levels, in predicting the offset and drift performance of an operational amplifier.

Errors Due to Finite Input Impedance

The prior discussions have presumed that open loop input impedance is infinite. Actually, solid state operational amplifiers have input impedances which range from 100 KΩ to several MΩ. In most applications it is reasonable to neglect the effects of finite input impedance; however, in instances where the summing impedance, R_i, is comparable to or larger in value than the amplifier input impedance, the closed loop performance of the circuit is somewhat degraded. The primary effect of finite input impedance is to reduce loop gain.

The degradation in close loop performance due to finite input impedance is best explained in terms of feed-

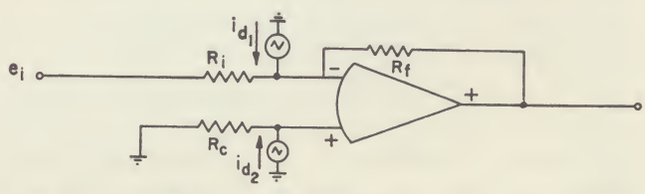


Fig 18 — Current drift compensation.

R_i KΩ	Δe_i due to e_d μV/°C	Δe_i due to i_d μV/°C	Total Δe_i μV/°C
1	25	0.5	25.5
10	25	5	30
100	25	50	75
1000	25	500	525

Fig 19 — Comparison of voltage and current source drift.

back attenuation (β): The circuit Fig 20 shows an amplifier with finite input impedance.

The calculation for β from eq (11) must be modified to account for the fact that Z_{IN} appears in parallel with Z_i in the feedback voltage divider.
If we let,

$$Z_x = Z_i \; Z_{IN}/(Z_i + Z_{IN}) \tag{19}$$

then from eq (11),

$$(\Delta e_o/\Delta e_i)(Z_x + Z_f)/Z_x = 1 + Z_f/Z_x = 1/\beta'$$

or

$$\beta' = \frac{1}{1 + (Z_f/Z_x)} \tag{20}$$

When Z_i becomes comparable to or higher in value than Z_{IN}, the value for feedback attenuation and consequently loop gain, Aβ′, is substantially reduced. For example, if a one megohm summing resistor were used with an amplifier with 100 KΩ input impedance, loop gain would be attenuated by approximately a factor of ten.

Fig 21 shows the effect of Z_{IN} on loop gain. A less obvious effect of finite input impedance is that the attenuation in loop gain also reduces closed loop bandwidth.

Finite Z_{IN}, does not affect closed loop gain, except by the increased errors due to reduced loop gain.

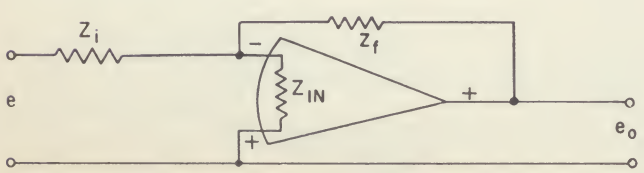


Fig 20 — Amplifier with finite input impedance.

Closed Loop Input Impedance

For the inverting connection, Fig 20, the closed loop input impedance is almost exactly equal to the summing impedance, Z_i, since the summing voltage is at virtually zero voltage. To be exact, the input impedance for this connection is,

$$Z_{icl} = Z_i + \frac{(Z_{IN}Z_f)/(Z_{IN} + Z_f)}{1 + AZ_{IN}/(Z_{IN} + Z_f)}$$

In the non-inverting connection, Fig 22, negative feedback is used to produce extremely high input impedance.

Closed loop input impedance for this configuration is:

$$Z_{icl} = Z_{IN}(1 + A\beta)$$

Theoretically, it is possible to obtain fantastically high input impedance in this way. However, common mode impedance and leakage resistance associated with the wiring and connectors tends to limit the attainable input impedance to generally 100 MΩ except for special very high input impedance amplifiers.

Errors Due to Non-zero Output Impedance

Open loop output impedance, Z_o, varies from as little as a few ohms to as much as several thousand ohms, with the majority of solid state amplifiers having 100 to 500 Ω output impedance. Output impedance forms a voltage divider with the load and feedback impedance which effectively attenuates open loop gain, A, which in turn reduces loop gain. The exact expressions for open loop gain taking output impedance into account is:

$$A' = \frac{A + (Z_o/Z_f)}{1 + \left[\frac{Z_f + Z_L}{Z_f Z_L}\right] Z_o} \approx \frac{A}{1 + \left[\frac{Z_f + Z_L}{Z_f Z_L}\right] Z_o} \tag{22}$$

Normally, manufacturers specify open loop gain at rated load with the assumption that $Z_f > Z_L$ so that in effect, a value for A′ is given. Open loop gain will vary slightly as the load impedance is changed. However, from eq (9) this variation is reduced by the loop gain in closed loop operation.

Output impedance will also cause additional phase shift with a capacitance load which tends to introduce stability problems. The circuit in Fig 13 shows a technique for correcting this difficulty.

Negative feedback reduces open loop output impedance by a factor approximately equal to the loop gain. Quantitatively, closed loop output impedance is:

$$Z_{ocl} = \frac{Z_o}{1 + A'\beta'}$$

Errors Due to Noise

Noise can be considered as any spurious output which is not contained in the input signal. Drift is merely a special case for noise which occurs at very low frequencies. The analysis of drift and the equations given to predict drift referred to the input and output are equally applicable to high frequency noise signals. In the general case, noise, like drift, can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction as depicted in Fig 15. Like drift, the effect of current

noise is directly proportional to the summing impedance.

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the frequency band for the specification is given.

Sources of Noise: Noise may appear at a discrete frequency, such as 60 c/s. It is usually picked up by electrostatic or electromagnetic coupling to the power lines or ac power transformers. In a chopper stabilized amplifier, there is usually noise generated at the chopping frequency. This noise may be produced by insufficiently shielded chopper drive leads or through electrostatic coupling within the chopper itself.

Noise can also arise from man-made RF interference. For example, the opening of a relay contact handling an inductive load may radiate sufficient energy to cause pulses of more than one volt peak to be generated across a three foot length of wire several feet away from the noise-generating circuit. The induced noise generally appears in the form of ringing at a frequency determined by the inductance and capacitance of the conductor that acts as a receiving antenna. While this ringing may appear in the region of 10 to 100 Mc/s, it may result in a low-frequency pulse output from a dc amplifier.

Because the base to emitter diode of a transistor amplifier stage is a rectifying junction, an RF noise input can be converted to a dc output. Thus transistor amplifiers are occasionally found to produce an audio output when in the vicinity of a strong broadcast station or may produce an audio pulse output due to an arcing relay.

RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. You can prevent noise pick-up by adequate shielding and the use of low-pass filters on all incoming leads connected with very short wires. Such filters generally have to be isolated from the feedback loop by adequate resistance in series with the input or output lead.

Random or statistical noise is generated in semiconductors and other components within an amplifier. "White" noise is a particular distribution of random noise which contains equal amounts of energy in each cycle of bandwidth. Such noise when generated by a resistor is termed "thermal" noise. The noise voltage generated by a transistor is generally white in the medium-high frequency region and increases in its energy per cycle at extreme high and low frequencies. Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to minimize random noise.

Thermal Noise: Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons, which generates minute voltages in a random

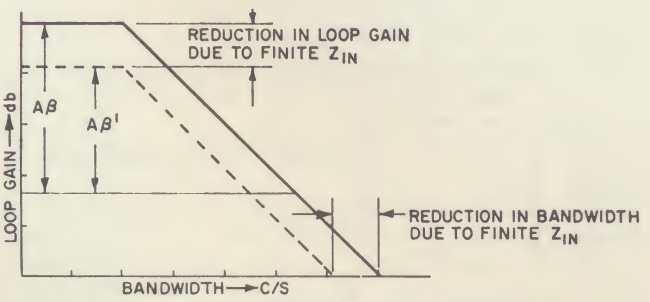


Fig 21 — Effect of Z_{IN} on loop gain and bandwidth.

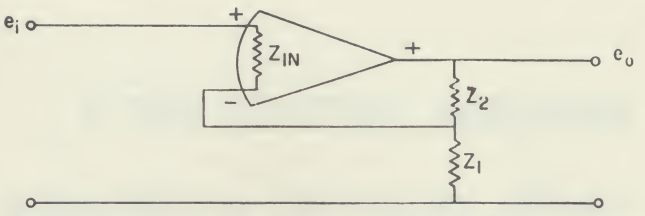


Fig 22 — Non-inverting connection for high input impedance.

manner across the terminals of the conductor or resistor. This noise voltage, sometimes referred to as "Johnson noise", is generated in the resistive component of any impedance and has a value:

$$E_n = \sqrt{4KT\,\Delta f R}$$

where E_n = the rms value of the noise voltage,
K = Boltzmann's Constant = 1.38×10^{-23} joules/°K,
T = absolute temperature of the resistance, °K,
Δf = the frequency band in which the noise is measured.

As a thumb rule, remember that a 1 kΩ resistor generates 1 μv rms in a 60 kc/s bandwidth. A 100 kΩ resistor generates 10 μv rms in the same bandwidth. The noise voltages generated by other values of resistance in other bandwidths can be calculated from these numbers by remembering that the noise is proportional to the square root of the resistance and the bandwidth.

Noise Specification: Although equivalent input noise voltage and noise current are most commonly used to characterize operational amplifier noise, there are several methods for specifying amplifier noise.

Equivalent Input Noise Voltage: It is convenient to separate the effects of equivalent input noise voltage and current. The equivalent input noise voltage of a dc amplifiers is that equivalent input noise voltage generated in series with a short circuit at the input terminals.

Equivalent Input Noise Current: When an amplifier is connected to a high impedance source, its noise output increases beyond that due to amplified noise voltage in the source resistance. When the source resistance becomes very large, the noise in a given bandwidth referred to the input becomes proportional to the source resistance. The increase in noise may be expressed in terms of an equivalent input noise current which causes a noise voltage drop across any large source resistance. Measurement of this noise current is generally made at such a high value of source resistance that the equivalent input noise voltage is much greater than that obtained with a shorted source.

Noise Figure: Noise figure is the ratio in db of the equivalent input noise power of the amplifier with a given source resistance over that noise power generated in the source resistance alone. For example, an amplifier having an equivalent input noise of 2 μv rms over a 60 kc/s bandwidth when connected to a 1 kΩ source resistor has a noise figure of 6 db because the equivalent input noise power is four times that of the source resistor alone.

Equivalent Input Noise Resistance: The equivalent input noise of an amplifier may be expressed in terms of the noise that would have been generated by a resistor connected in series with the input terminals of a noiseless amplifier. In the example above, the amplifier had an equivalent noise resistance of 3 kΩ which, when added to the source resistance of 1 kΩ, generated an equivalent input noise voltage of 2 μv rms. ■

OPERATIONAL AMPLIFIERS, PART II

Inverting, non-inverting and differential configurations

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Part I. Principles of Operation and Analysis of Errors appeared in the September issue of EMD.

Most operational amplifier circuits are constructed in one of three basic amplifier configurations—inverting, non-inverting or differential. The useful properties of all three configurations depend on the virtues of negative feedback coupled with extremely high open loop voltage gain. The configurations differ only in the manner in which the input signal is applied and the feedback components are arranged. The relative merits and limitations of these three basic configurations are discussed in this article.

INVERTING CONFIGURATION

The characteristics of the inverting configuration (Fig 23) were analyzed in Part I and will not be repeated here but a summary of the essential advantages and disadvantages is presented.

Highest accuracy can generally be obtained with the inverting amplifier, since, unlike the non-inverting amplifier, one input is normally grounded and there are no common mode voltage errors. Single ended amplifiers, which require that one input be grounded, can be used only in the inverting connection. This includes most chopper stabilized type operational amplifiers. For ac amplifiers you can obtain the lowest distortion in the inverting mode since common mode voltage errors also introduce distortion. The inverting configuration is excellent for summing two or more input signals. This follows as the summing junction is virtually at ground potential so that the input signals are almost completely isolated from each other.

Another versatile feature of the inverting amplifier is that it is possible to obtain closed loop gains less than one; which is not possible with the non-inverting amplifier. In many applications such as active filters, servo amplifiers and integrators you must attentuate a portion of the frequency response below unity gain.

Closed loop input impedance, for the inverting amplifier, which is essentially equal to the summing impedance, Z_1, is limited to a few megohms for all practical purposes. This follows, because as a rule of thumb, the summing impedance should not be much greater than the amplifier's open loop input impedance, Z_{IN}, which for most solid state operational amplifiers is in the range from 0.1 to 1 megohm. Another limitation is that the inverting configuration for very low closed loop gains degrades voltage source drift and noise by as much as a factor of two for unity gain. This degradation in drift and noise does not occur for the non-inverting configuration. The inverting configuration is a poor choice if you require both high input impedance and wide bandwidth. When using large summing and feedback resistors, stray capacitance has a greater effect in limiting closed loop bandwidth.

Low Input Impedance

Negative feedback reduces the input impedance at the summing junction of the inverting amplifier to negligible proportions. You can use this characteristic to advantage in some applications such as amplifying the output from photocells and other current generator type transducers. In analyzing circuits of this type it is convenient to treat the input signal as a current source as shown in Fig 24. Closed loop gain from a current source with infinite source impedance, is:

$$e_o/i_s = -(Z_f)\frac{1}{1+1/A\beta} \approx -Z_f \text{ for } A\beta >> 1$$

$$\text{where } 1/\beta = 1 + \frac{Z_f}{Z_{IN}} \text{ and } A \text{ is the open loop gain.} \quad (23)$$

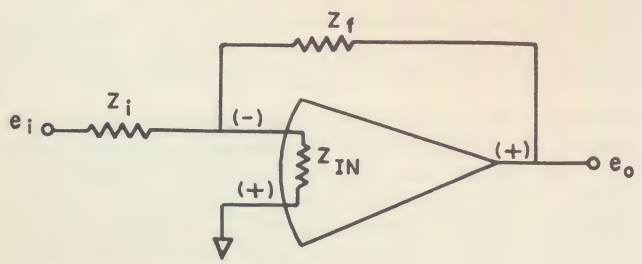


Fig 23 — Inverting configuration.

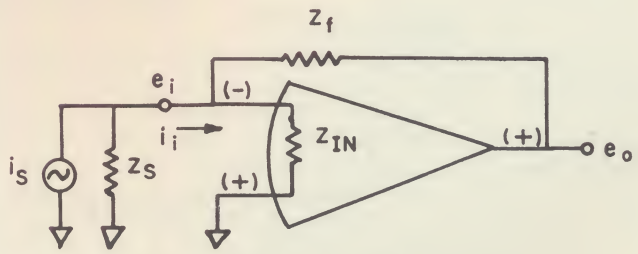


Fig 24 — Current source amplifier.

We see that if loop gain, Aβ, is sufficiently large, the value of the feedback resistor, Z_f entirely determines the gain. Closed loop input impedance is:

$$Z_i = \frac{e_i}{i_i} = \frac{\left(\frac{Z_f \cdot Z_{IN}}{Z_f + Z_{IN}}\right)}{(1 + A\beta)} \qquad (24)$$

When the source impedance, Z_s, becomes equal to or less in value than the open loop input impedance Z_{IN}, in parallel with the feedback impedance Z_f, you attenuate loop gain For finite, Z_s, modify eqs (23) and (24) by substituting $1/\beta'$ for $1/\beta$ where:

$$1/\beta' = 1 + \frac{Z_f(Z_s + Z_{IN})}{Z_s Z_{IN}} \qquad (25)$$

The effect of voltage and current drift for the circuit in Fig 24 is more revealing when referred to the output. Drift at the output is:

$$\Delta e_o = e_d\left(\frac{Z_s + Z_f}{Z_s}\right) + i_d Z_f \qquad (27)$$

where e_d is the voltage source drift, i_d is the current source drift.

NON-INVERTING CONFIGURATION

The most useful property of the non-inverting amplifier is the extremely large input impedance developed by negative feedback. Consequently, this configuration is most usful as a buffer or impedance transformation amplifier and for amplifying signals from very large source impedances.

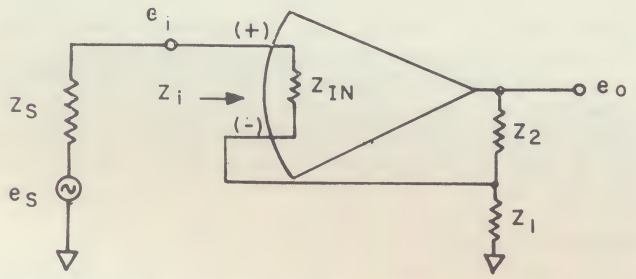


Fig 25 — Non-inverting configuration.

In this configuration, the input signal feeds to the non-inverting input and feedback returns to the inverting input as shown in Fig 25. Since negative feedback maintains the error voltage between the amplifier inputs to an infinitesimal value, you see that the negative input must follow any changes applied to the positive input. Therefore, the successful performance of this circuit requires a differential input amplifier where both inputs can operate above ground potential and where the rejection of common mode voltage is very good. Since most chopper stabilized operational amplifiers are single ended, you can not use them in this circuit.

Closed Loop Input Impedance

The high input impedance of the non-inverting connection is due to what is basically potentiometric feedback where the output signal or some fraction thereof is summed in series with the input. Consequently, the only input current which flows is due to the error voltage

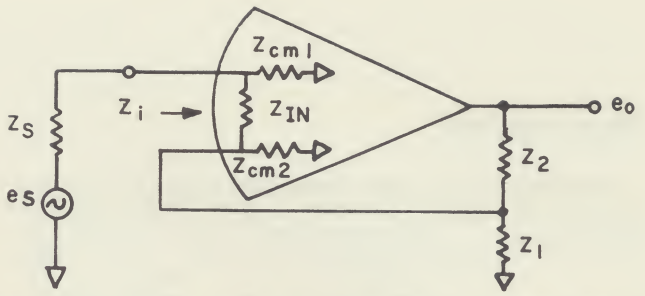


Fig 26 — Non-inverting amplifier with common mode input impedance.

across the amplifier's open loop input impedance Z_{IN}. Quantitatively, eq (28) gives the closed loop impedance if you assume that Z_{IN} is greater than the parallel impedance of Z_1 and Z_2.

Then,

$$Z_i = Z_{IN}\left[1 + A\beta\right] = Z_{IN}\left[1 + A\left(\frac{Z_1}{Z_1 + Z_2}\right)\right] \qquad (28)$$

Notice from eq (28) that Z_i depends only on the ratio of $Z_1/(Z_1 + Z_2)$. Therefore, the magnitudes of Z_2 and Z_1 can be quite low without affecting input impedance, their magnitude being limited only by the output current rating of the amplifier. This situation offers two distinct advantages as compared to the inverting amplifier. First, for circuits requiring high gain and high input impedance, you can select resistors in a range of values where high quality, stable components are readily available. Secondly, you can design high input impedance, wideband amplifiers since stray capacitance has a smaller effect with the relatively low impedances which can be used for the feedback components.

From eq (28) you would expect input impedance to approach infinity as open loop gain, A, becomes very large. This would be true if it were not for common mode input impedance. In addition, to the impedance between amplifier inputs, Z_{IN}, there is also an effective impedance from each input to ground as shown in Fig 26. The parallel sum of the impedances from each input to ground, generally specified as the common mode input impedance, is Z_{cm} where:

$$Z_{cm} = \frac{Z_{cm1} \cdot Z_{cm2}}{Z_{cm1} + Z_{cm2}}$$

For transistor type differential amplifiers, common mode impedance generally ranges from 10 to 500 megohms and it is this value which sets the upper limit on the closed loop input impedance, Z_i, which can be achieved in the non-inverting configuration. Note that the output supplies the current for Z_{cm2} so that only Z_{cm1} draws input current. Therefore, the expected limit on closed loop impedance would be twice the specified common mode impedance, Z_{cm}.

At high frequencies three factors pose additional limits on the achievable input impedance.

- Lower open loop gain at higher frequencies reduces the negative feedback which causes the high input impedance.
- Shunt capacitance across the inputs reduces open loop input impedance at high frequencies.
- Shunt capacitance to ground reduces common mode impedance at high frequencies.

Closed Loop Gain

Assuming infinite input impedance, closed loop gain is:

$$\frac{e_o}{e_s} = \underbrace{\left[\frac{Z_1 + Z_2}{Z_1}\right]}_{\substack{\text{ideal} \\ \text{amplifier}}} \underbrace{\left[\frac{1}{1 + 1/A\beta}\right]}_{\substack{\text{error due to} \\ \text{finite gain}}}$$

$$\approx \left(\frac{Z_1 + Z_2}{Z_1}\right)\left(1 - 1/A\beta\right) \qquad (29)$$

where $1/\beta = (Z_1 + Z_2)/Z_1$ is the ideal closed loop gain, A is the open loop gain and the factor $A\beta$ is the loop gain. As for the inverting configuration, gain error is inversely proportional to loop gain. Eq (29) shows that with infinite $A\beta$, you cannot attenuate the closed loop gain below unity for any frequency. Unity gain occurs when $Z_1 = \infty$ and $Z_2 = 0$.

Gain for finite open loop input impedance, Z_{IN}, is,

$$\frac{e_o}{e_s} = \left[\frac{Z_1 + Z_2}{Z_1}\right]\left[\frac{1}{1 + 1/A\beta'}\right]$$

$$\text{where } 1/\beta' = \left(\frac{Z_1 + Z_2}{Z_1}\right)\left(\frac{Z_{IN} + Z_s}{Z_{IN}}\right) \qquad (30)$$

Consideration of common mode input introduces a further error in the closed loop equation. To a first approximation you should look at the effect of common mode impedance as forming a voltage divider to ground with source impedance, Z_s. This case modifies the gain equation to:

$$\frac{e_o}{e_s} = \left(\frac{Z_1 + Z_2}{Z_1}\right)\left(\frac{2Z_{cm}}{2Z_{cm} + Z_s}\right)\left(\frac{1}{1 + 1/A\beta'}\right) \qquad (31)$$

Common Mode Voltage Errors

Common mode voltage rejection is a source of error for the non-inverting configuration which is not a problem for the inverting connection. Ideally, for a differential input amplifier, the gain from each input to the output is exactly equal and opposite so that no output is produced when the same voltage is applied to both inputs. When the gains of each input are not exactly balanced, an output will be produced for a common mode input voltage. This output error, generally referred to the input as a ratio of the applied common mode voltage, is the common mode rejection ratio (CMR).

Since both inputs of a non-inverting amplifier assume approximately the same voltage, you would expect an input error equal to the CMR times the input voltage. The limit of the maximum input voltage is generally specified as the maximum common mode voltage.

Voltage Drift and Offset

Unlike the inverting amplifier, input voltage source drift (and noise) referred to the source voltage is independent of closed loop gain for the non-inverting amplifier. Thus for unity gain, voltage drift is improved by a factor of two as compared to the inverting amplifier.

Current Drift and Offset

The effect of current source offset and drift depends primarily on the magnitude of the source impedance. As shown in Fig. 27 offset current required by the plus input must be drawn through the source resistance. This produces an input offset voltage proportional to the product of offset current, i_d, and the source resistance, Z_s.

$$\Delta e_s \doteq i_d Z_s$$

For very large source impedance, the magnitude of initial offset current and current drift is a very important consideration in selecting an amplifier. For example, an amplifier with any initial offset current of 10 na and current drift of 1 na/°C when used with a source impedance of

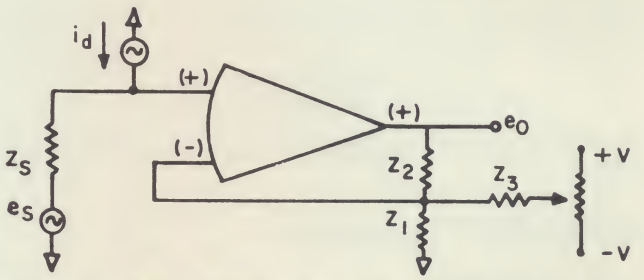


Fig 27 — Balance circuit for offset current ($Z_3 >> Z_1$).

10 megohms will produce an input offset voltage of 100 mv and drift of 10 mv/°C.

To bias out the initial offset current, sum an equal and opposite current to the non-inverting input as shown in Fig 28. However, the biasing network used in this scheme tends to lower the input impedance. Fig 27 shows a preferred circuit for zeroing large voltage offset due to input current which does not affect input impedance.

It is important to realize that the external zero voltage adjustment provided with many amplifiers is intended for balancing the amplifier's initial offset voltage and it should not be used to compensate for large voltage offsets due to offset current. The reason is that you may increase drift by intentionally generating a large voltage offset within the amplifier to compensate for current offset.

To reduce the effect of initial current offset and drift in some cases, add a resistance equal to the source impedance in series with the inverting input. Since offset current at each input is generally about equal and tends to track with temperature change, equalizing the impedance in both input leads cancels the effects of current drift to the extent that the input currents track. The limitation here is that as Z_s becomes greater than the open loop input impedance Z_{IN}, loop gain is lost. Moreover, large impedance in the inverting input tends to restrict the bandwidth due to stray capacitance and to generate excessive noise.

For the inverting amplifier, drift errors due to current offset, i , increase proportional to closed loop input impedance, since the summing impedance, Z , determines both the input impedance and the drift errors ($i\ Z$). However, for the non-inverting amplifier drift errors due to current offset is only a function of the source impedance ($i\ Z$) and is independent of closed loop input impedance. Usually the non-inverting amplifier is considered as a means of obtaining higher input impedance, but from this analysis we can see that another and equally important consideration by selecting the non-inverting configuration is to obtain lower overall drift errors for a given source impedance.

Non-Inverting ac Amplifier

When a blocking capacitor is used to ac couple the input to the non-inverting amplifier, a dc path must be provided for the input current as shown in Fig 28. Returning the leakage resistor to ground or preferably to a bias voltage, generates an equal and opposite current to null the initial offset current. The closed loop gain amplifies any offset voltage developed by input current to produce an output offset which tends to limit the output dynamic range. The maximum value for use for leakage resistance, R_L, is limited by the magnitude of current drift, the closed loop gain and the required output dynamic range.

Limitations on Maximum Source Impedance

Several factors have been mentioned which limit the maximum source impedance which can be used with a given set of amplifier specifications. The major considerations are:

- Loop gain is attenuated when the source impedance exceeds the amplifier's open loop input impedance, Z_{IN}. The magnitude of this attenuation is $Z_{IN}(Z_{IN} + Z_s)$. Gain accuracy, gain stability and closed loop input impedance are all degraded by loss of loop gain.
- The effect of input current noise is proportional to the magnitude of source impedance and excessive input noise can be generated for very large Z_s.

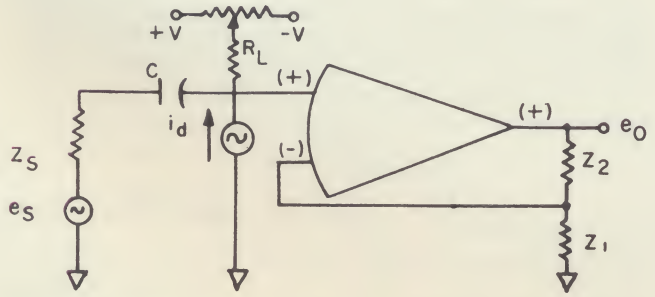


Fig 28 — AC non-inverting, with current offset adjust.

- Input voltage drift is produced which is proportional to the product of source impedance and current source drift.
- When the source impedance, Z_s, becomes comparable to or greater than the common mode impedance, Z_{cm}, an additional error is introduced into the closed loop gain; the error factor being:

$$\frac{2\ Z_{cm}}{2\ Z_{cm} + Z_s}$$

In conclusion, open loop input impedance, both common mode and differential, current source drift, noise and offset and open loop gain are the principle amplifier specifications which limit the maximum source impedance which can be used with the non-inverting configuration.

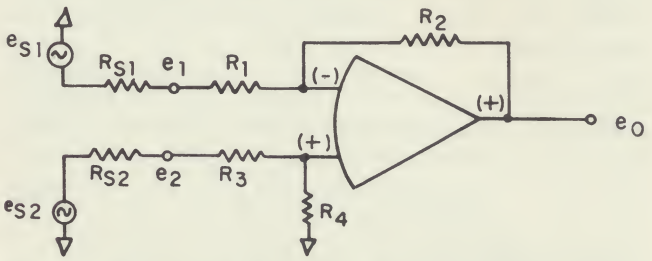


Fig 29 — Differential configuration.

DIFFERENTIAL CONFIGURATION

Ideally, the differential configuration shown in Fig 29 amplifies only the potential difference between e_1 and e_2. Voltages of the same potential, so-called common mode voltage, are not amplified. This configuration is useful in such applications as amplifying signals which are floated above ground potential, substracting voltages and measuring resistance bridge signals. The circuit can also amplify small signals in the presence of common mode noise voltage. Closed loop gain, for an infinite gain amplifier is:

$$e_o = e_2\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) - e_1\left(\frac{R_2}{R_1}\right) \qquad (33)$$

Except in applications, such as substracting, which require a scale factor difference, adjust the ratios R_2/R_1 and R_4/R_3 to be equal. In this case eq (33) becomes:

$$e_o = \left(\frac{R_2}{R_1}\right)(e_2 - e_1) \text{ for } \frac{R_1}{R_2} = \frac{R_3}{R_4} \qquad (34)$$

Closed loop input impedance for e_1 is just the summing resistor, R_1, while for e_2 it is $(R_3 + R_4)$. Like the inverting amplifier, the differential amplifier sometimes suffers from the relatively low input impedances which can be achieved. Fig 30 shows one arrangement of amplifiers which combines the high input impedance of the non-inverting amplifier with the common mode rejection capabilities of the differential amplifier. Gain for this circuit is:

$$e_o = \left(1 + x + y\right)\frac{R_2}{R_1}(e_2 - e_1) \qquad (35)$$

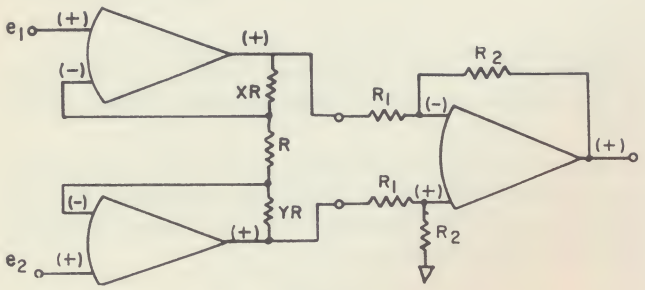


Fig 30 — Circuit for differential, high input impedance.

Common Mode Voltage and Rejection Ratio

The circuit of Fig 29 requires a differential input type amplifier where both inputs are operable above ground potential and where the rejection of common mode voltage at the two inputs is very good. Both inputs are constrained by negative feedback to be at essentially the same potential which is (e_2) ($R_4/R_3 + R_4$). If we call E_{cm} the maximum common mode voltage which the amplifier input terminals can withstand, then the maximum common mode voltage which can be applied to e_1 end e_2 is,

$$e_{1,2}\ max. = E_{cm}\frac{R_3 + R_4}{R_4} \qquad (36)$$

Common mode rejection ratio (CMR) is defined as the applied common mode voltage divided by the resulting error referred to the input. CMR for the circuit in Fig 29 depends on several factors which are discussed separately below. We shall assume here that $R_1 = R_3$ and $R_2 = R_4$.

Source Impedance Unbalance: An unbalance in source impedance will cause a common mode voltage error. The CMR, due to a small unbalance in source impedance is:

$$CMR = \frac{R_{s2} + R_3 + R_2}{(R_{s1} + R_1) - (R_{s2} + R_3)} \qquad (37)$$

$$For\ R_1 = R_3,\ R_2 = R_4,\ R_{s1} = R_s,\ R_{s2} = R_s - \Delta R_s$$

$$and\ R_s >> \Delta R_s$$

$$CMR \approx \frac{R_s}{\Delta R_s}\left(1 + \frac{R_1 + R_2}{R_s}\right)$$

Hence a given percentage unbalance in R_s will have a smaller effect on CMR when $(R_1 + R_2) >> R_s$.

Summing Impedance Mismatch: A common mode error is also introduced by a mismatch in the summing impedances, R_1 and R_3. Use eq (37) to predict the CMR due to this mismatch. Assuming $R_{s1} = R_{s2} = R_s$, $R_3 = R_1 - \Delta R_1$, and $R_1 >> \Delta R_1$, then eq (37) becomes:

$$CMR \approx \frac{R_1}{\Delta R_1}\left(1 + \frac{R_s + R_2}{R_1}\right)$$

Feedback Impedance Mismatch: A mismatch in R_2 and R_4 will cause a common mode voltage error for which CMR is given by eq (38).

$$CMR = \left(\frac{R_1 + R_4 + R_{s1}}{R_4 - R_2}\right)\left(\frac{R_2}{R_1 + R_{s1}}\right) \qquad (38)$$

Assuming

$$R_{s1} = R_{s2} = R_s,\ R_4 = R_2 + \Delta R_2\ and\ R_2 >> \Delta R_2$$

then eq (38) becomes,

$$CMR = \frac{R_2}{\Delta R_2}\left(1 + \frac{R_1 + R_s}{R_2}\right)\left(\frac{R_2}{R_1 + R_s}\right) \qquad (39)$$

From eq (39) we see that a circuit with higher gain, R_2/R_1, will have a higher CMR for a given percentage unbalance, $R_2/\Delta R_2$.

Amplifier Common Mode Rejection: The inherent common mode rejection of the amplifier itself will limit the common mode rejection of the circuit to that of the amplifier. Note that unbalancing the resistors R_1 and R_3, or R_2 and R_4, cancels the common mode error and effectively increases the CMR to infinity. The residual signal due to a common mode voltage will then consist of only distortion components arising in the input stage of the amplifier as it swings over the common mode voltage range.

AC Common Mode Rejection: When used to reject ac common mode voltages, unbalance of stray capacitance between each input and ground can cause a common mode voltage error. CMR due to stray capacitance is given by:

$$CMR = \frac{(R_p + jX_1)(R_p + jX_2)}{R_p(jX_1 - jX_2)} \qquad (40)$$

where $R_p = R_1R_2/(R_1 + R_2)$, jX_1 is the reactance to ground from input e_1 due to stray capacitance and jX_2 is the reactance to ground from input e_2.

Voltage and Current Drift

Offset and drift for the differential configuration are very much the same as for the inverting configuration which was discussed in Part I Sept EMD. In most differential amplifiers, the parallel sum of the impedances from each input to ground is balanced. Since the current at each input tends to track the other with changes in temperature, voltage offset due to current drift is cancelled to the extent that the currents do track.

OPEN LOOP OPERATION AND VOLTAGE COMPARATORS

In some applications you use the extremely high sensitivity of operational amplifiers, due to high open loop gain, with little or no feedback. In this case, the operational amplifier operates basically as a switch, since output is saturated at either the maximum positive or negative output voltage and a very small input voltage will cause the output to change polarity. Voltage comparators, used in digital voltmeters, analog-to-digital converters and precise timing circuits, are the most common application of operational amplifiers in the open loop mode. Fig 31 shows a simplified circuit for a voltage comparator.

The input signal, e_1, and the reference signal, e_{ref}, must be of opposite polarities. As the input voltage exceeds the reference voltage, a very small difference will cause the output to rapidly switch polarity. The threshold, or volt-

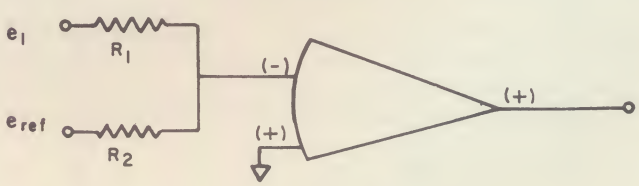


Fig 31 — Voltage comparator circuit.

age difference required to switch the output, depends on the maximum swing of the output voltage and the open loop gain of the amplifier. For example, if the maximum output swing were ±10 v and the open loop gain were 100,000, a 100 μv difference between the input and reference voltage would switch the output polarity. For a 100 v reference signal, this gives the circuit the ability to compare voltages to within one part in 10^6.

If you slowly vary the input voltage, any noise appearing on the input signal, the reference voltage or any noise picked up by the summing junction or generated within the amplifier itself will cause the output to chatter at the time of coincidence. Fig 32 shows how to eliminate this chattering by the use of positive feedback, which provides a hysteresis exceeding the noise level.

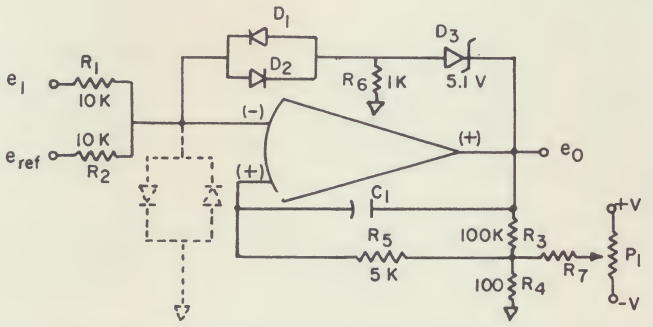


Fig 32 — Voltage comparator with hysteresis ($R_7 >> R_4$).

The zener diode feedback limits the amplifier output swing to —0.5 to 5 v. As the input voltage approaches the trigger level, the regenerative feedback due to switching the output causes a step in the net voltage of the positive input equal to one-thousandth of the output voltage change, or 5.5 mv. If the input noise level is less than 5.5 mv peak-to-peak, there will be no chattering of the output as a result of noise for a monotonic change of e_1 due to the bias generated at the positive input. Adjust the amount of hysteresis by changing the zener diode voltage or the ratio of R_3 and R_4. Add the resistor, R_5, in the positive input to balance the impedances of both amplifier inputs to ground, thereby reducing input offset due to current drift. Use the bias circuit formed by R_7 and P_1 to zero initial input offset.

Diodes D_1 and D_2 reduce leakage current to the summing junction which is generated by the zener diode, D_3. To some extent, depending on the values of R_2, R_6 and e_{ref}, these diodes also protect the summing junction from overloads. However, for very large reference voltage and small R_2 it may be desirable to add a pair of low leakage silicon diodes from the summing junction to ground to prevent damage or saturation of the amplifier input for large unbalance between the input signal and the reference voltage. With protecting diodes to ground and stable summing resistors, excellent performance is possible with hundreds of volts unbalance. The clamping feedback circuit also prevents the amplifier from saturating which guarantees rapid recovery in switching the output. The capacitor, C_f, speeds the switch action of the regenerative feedback and improves closed loop stability for some amplifier types.

Errors In Comparator Circuits

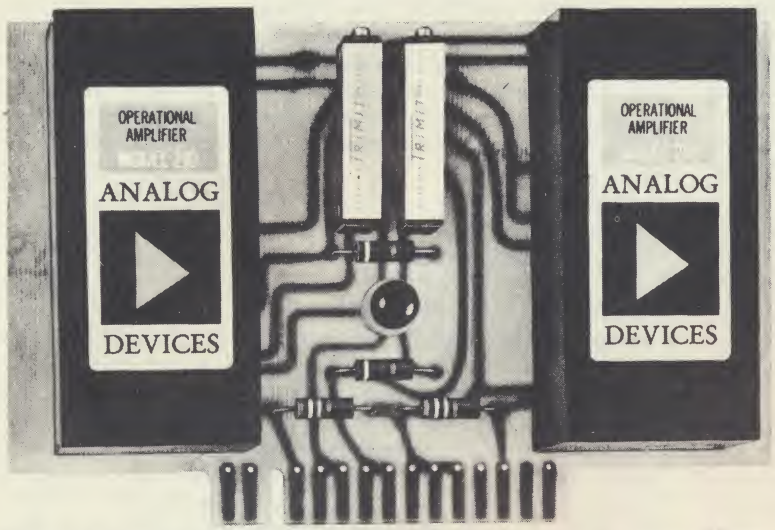
We have already mentioned that one error in the comparator's operation is the amount of error voltage required at the summing junction to switch the output. Most operational amplifiers have sufficient open loop gain so that this error is small compared to that due to noise and drift. Noise for obvious reasons limits the threshold of comparison and hysteresis should be used which is greater than the peak-to-peak noise at the summing junction from all sources including the signal and reference voltages.

Input offset drift, of course, shifts the level of coincidence between the input signal and the reference signal and thereby introduces an error in the absolute voltage as well as the repeatability of comparison. The factors contributing to input offset drift are the same as though the amplifier were used as a linear inverting amplifier and can be predicted from the amplifier's specifications and other considerations previously discussed. The same techniques that minimize drift in linear dc amplifier circuits should be used in comparator circuits. Namely, the summing impedance should be as low as possible, the impedances of each input of a differential amplifier should be balanced and summing impedances greater than the open loop input impedance of the amplifier should be avoided. With differential type amplifiers, noise and drift errors below 1 mv can be readily obtained and with chopper stabilized amplifiers, errors less than 50 μv are possible. Frequently these low errors are exceeded by noise and drift in the input and reference signals.

Response Time

When the input signal is changing rapidly through the trigger point, there may be a delay in the output switching due to the frequency response characteristics of the amplifier. While you can sometimes compensate the delay by a change in the reference voltage, this delay is frequently a function of temperature. For this reason, you obtain best high speed operation with amplifiers having wide gain bandwidth. Actually slewing rate or, alternatively, full output voltage response is the most significant specification, since rate limiting generally restricts the response time.

Overload recovery time can also introduce a delay in response. Therefore, the amplifier used must either have very fast recovery time or a circuit like that in Fig 32 must be used which prevents output overload and therefore any delay due to overload recovery. ■



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